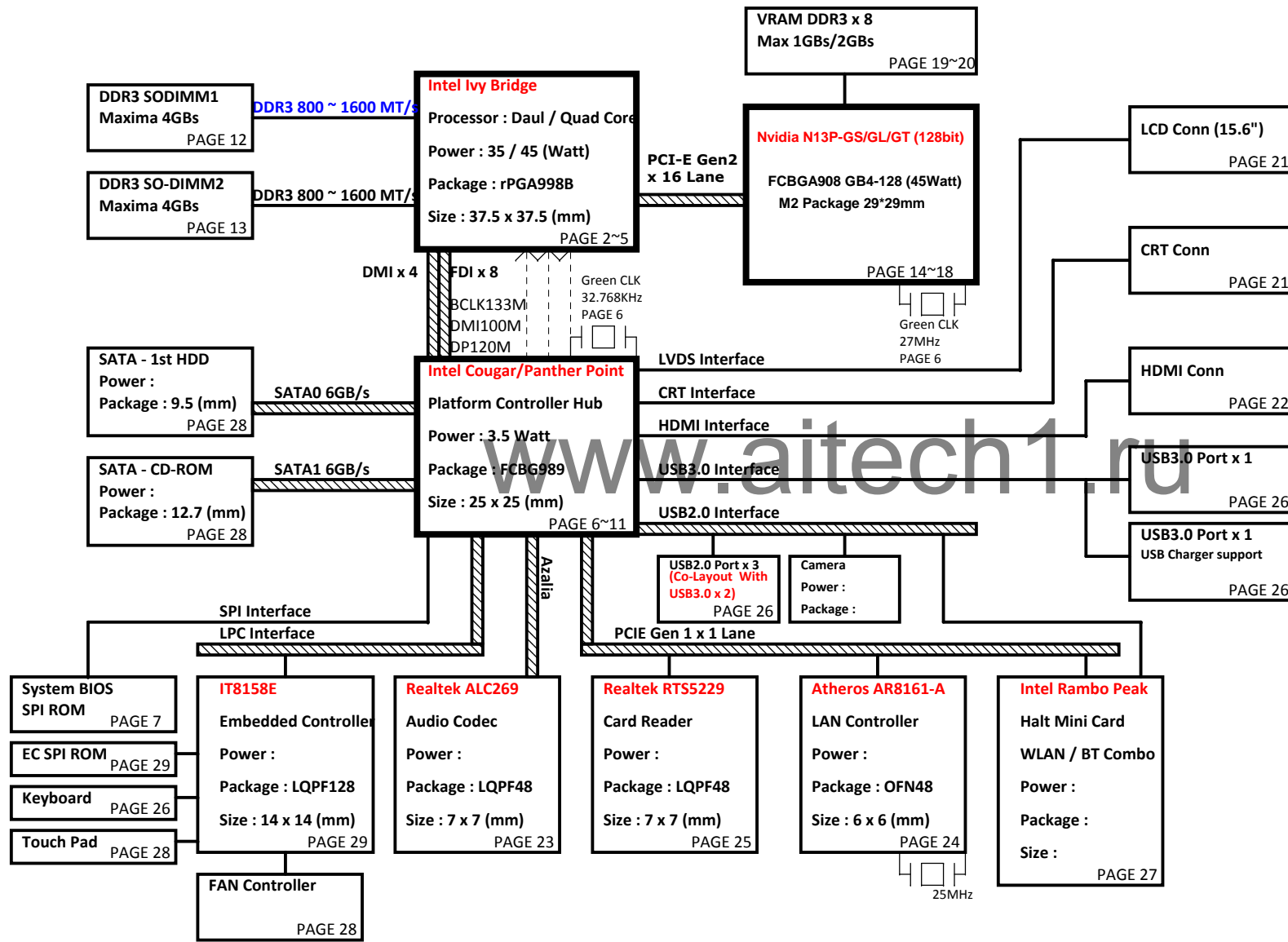


# (15.6") Intel Chief River Platform Block Diagram



## PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT

## PCB 8L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : IN3(High)  
LAYER 7 : SGND2  
LAYER 8 : BOT

## Power Source

### O2Micro OZ8681

System Charge Power (+BATCHG)

### P2806

System Discharge Power  
(+1.5V/+3V/+5V)

### Ricktek RT8205

System Power (+3VPCU/+5VPCU/  
+3V5S/+5V5S)

### NCP6131/NCP5911/RT8209/G9334

Processor Power (+VCC\_CORE/  
+1.05\_VTT/+VCCSA)

### Richtek RT8207

System Memory Power (+1.5VSUS/  
+0.75V\_DDR\_VTT)

### Richtek RT8209/RT9025

PCH Power (+1.05/+1.8V)

### O2Micro OZ8122

DGPU Power (+VGACORE/+3.3V\_GFX/  
+1.8\_VGA/+1.5\_GFX/+1.05\_GFX)



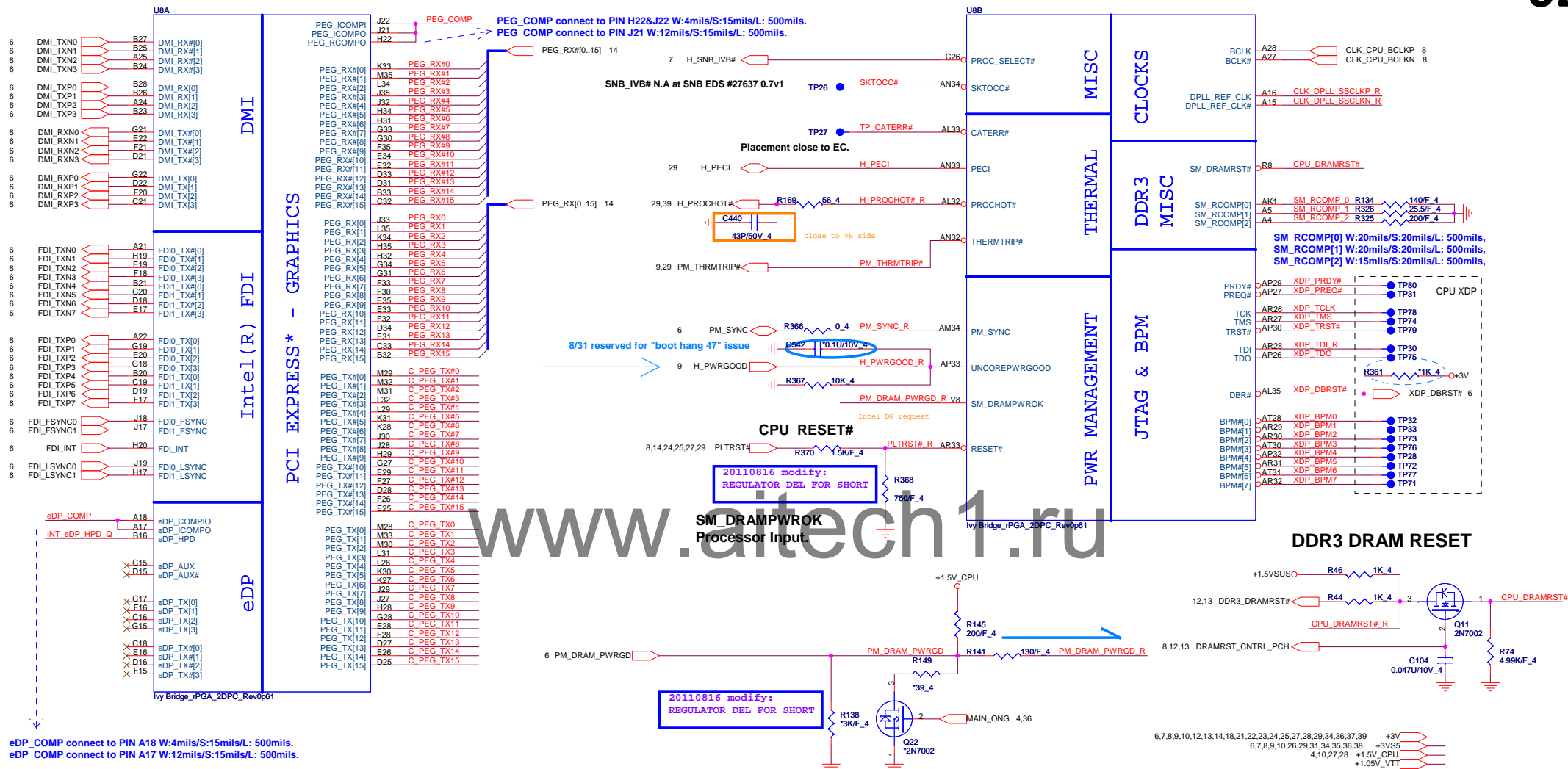
**PROJECT : TWC**  
**Quanta Computer Inc.**

Size  
A3

Document Number  
**Block Diagram**

Rev  
A

Date: Monday, November 07, 2011 Sheet 1 of 40

FDI disable  
(DIS only stuff)20110816 modify:  
FDI DEL FOR SGFDI\_FSYNC can gang all these 4  
signals together and tie them  
with only one 1K resistor to GND  
(DG V0.5 Ch2.2.9).

## PEG x16 disable (UMA only remove)

C_PEG TX0	C_PEG TX1	C_PEG TX2	C_PEG TX3	C_PEG TX4	C_PEG TX5	C_PEG TX6	C_PEG TX7	C_PEG TX8	C_PEG TX9	C_PEG TX10	C_PEG TX11	C_PEG TX12	C_PEG TX13	C_PEG TX14	C_PEG TX15
C564	C565	C566	C567	C568	C569	C570	C571	C572	C573	C574	C575	C576	C577	C578	C579

0.22uF AG coupling Caps for PCIE GEN3

C_PEG TX0	C_PEG TX1	C_PEG TX2	C_PEG TX3	C_PEG TX4	C_PEG TX5	C_PEG TX6	C_PEG TX7	C_PEG TX8	C_PEG TX9	C_PEG TX10	C_PEG TX11	C_PEG TX12	C_PEG TX13	C_PEG TX14	C_PEG TX15
C580	C581	C582	C583	C584	C585	C586	C587	C588	C589	C590	C591	C592	C593	C594	C595

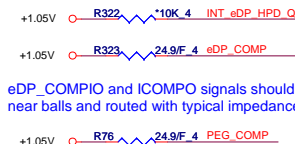
0.22uF AG coupling Caps for PCIE GEN3

## Embedded Display PLL Clock

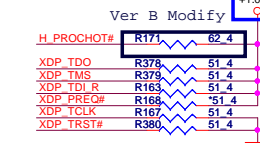


20110816 CLK DPLL\_SSCLK DEL

## DP &amp; PEG Compensation

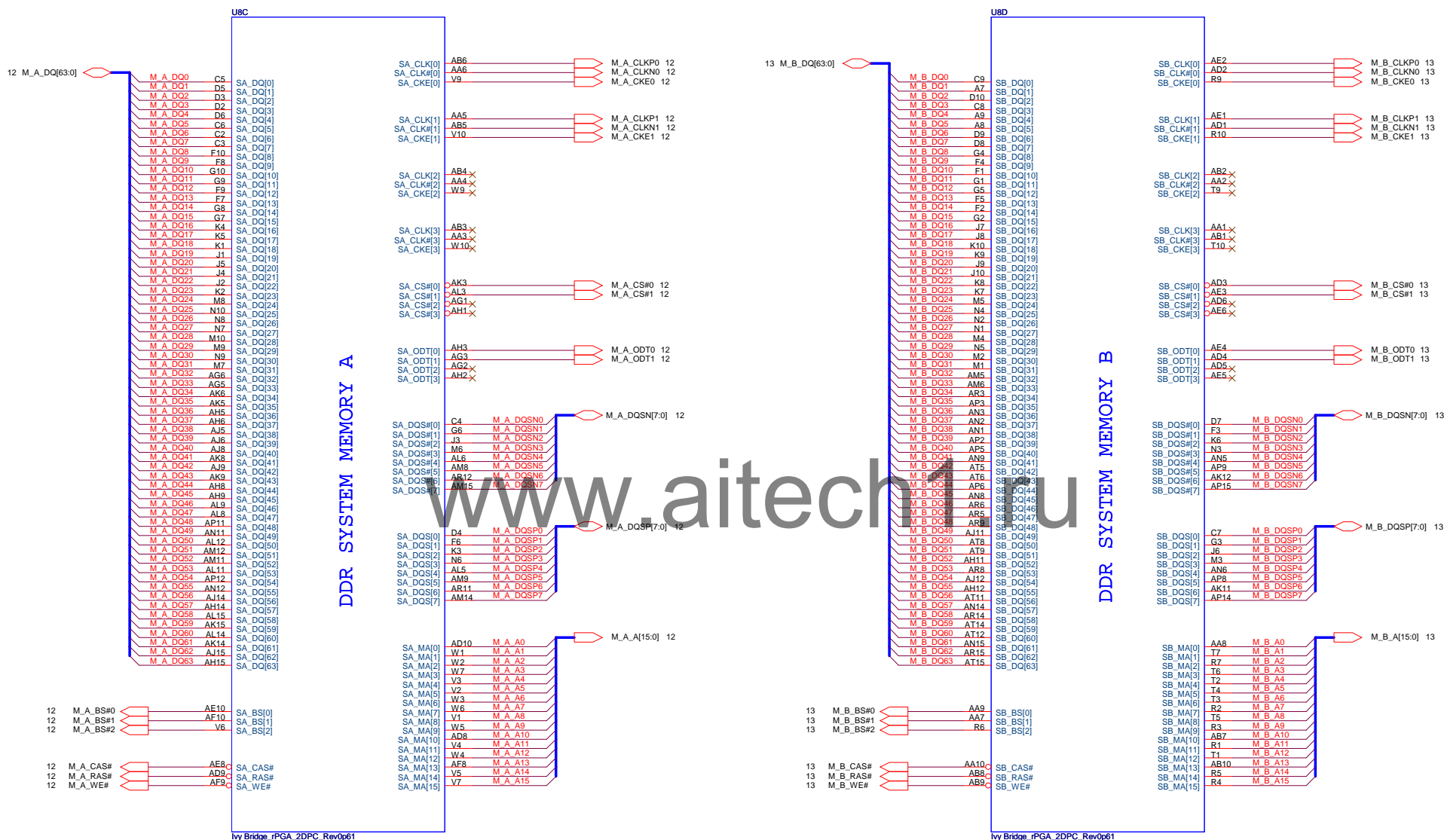
eDP\_COMPIO and ICOMPO signals should be shorted  
near balls and routed with typical impedance <25 mohmsPEG\_ICOMPI and RCOMPO signals  
should be routed within 500 mils typical  
impedance = 43 mohms PEG\_ICOMPO  
signals should be routed within 500 mils  
typical impedance = 14.5 mohms

## Processor pull-up (CPU)

PROJECT : TWC  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 1/4 (Host/GPU)	A
Date: Monday, November 07, 2011	Sheet 2 of 40	

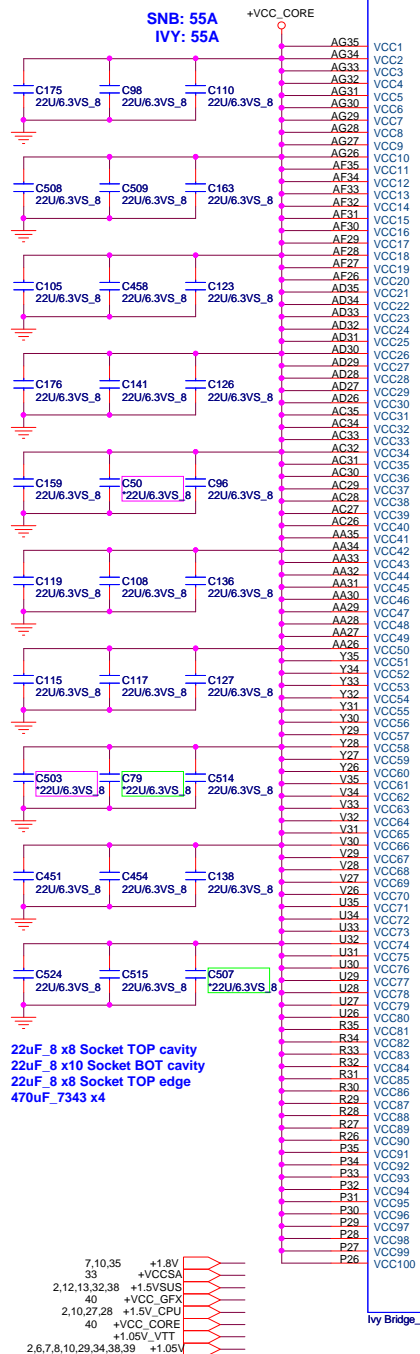
## Ivy Bridge Processor (DDR3)



## Ivy Bridge Processor

## POWER

U8F



PEG AND DDR

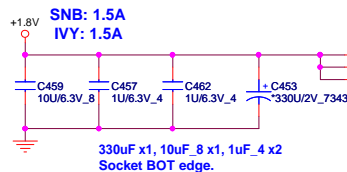
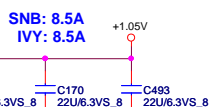
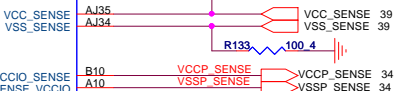
CORE SUPPLY

SVID

SENSE LINES

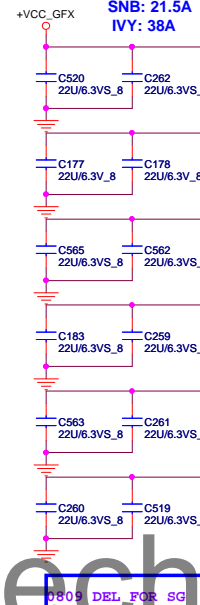
VIDALERT#  
VIDSCLK  
VIDSOUT

AJ29 H\_CPU\_SVIDALRT#  
AJ30 VR\_SVID\_CLK  
AJ28 H\_CPU\_SVIDDAT



22uF\_8 x2 Socket TOP cavity  
22uF\_8 x2 Socket BOT cavity  
22uF\_8 x4 Socket BOT edge  
470uF\_7343 x2

**SNB: 21.5A  
IVY: 38A**



## POWER

U8G

GRAPHICS

1.8V RAIL

Ivy Bridge\_PGA\_2DPC\_Rev0p61

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

VAXG\_SENSE  
VSSAXG\_SENSE

SM\_VREF

SA\_DIMM\_VREFDQ  
SB\_DIMM\_VREFDQ

VDDQ1  
VDDQ2  
VDDQ3  
VDDQ4  
VDDQ5  
VDDQ6  
VDDQ7  
VDDQ8  
VDDQ9  
VDDQ10  
VDDQ11  
VDDQ12  
VDDQ13  
VDDQ14  
VDDQ15

VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8

VCCSA\_SENSE  
VCCSA\_VID[0]  
VCCSA\_VID[1]  
VCCIO\_SEL

VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8

VCCSA\_SENSE  
VCCSA\_VID[0]  
VCCSA\_VID[1]  
VCCIO\_SEL

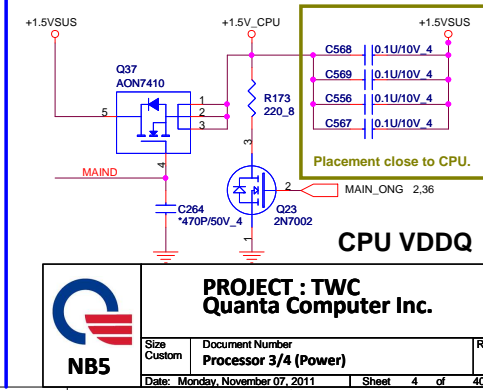
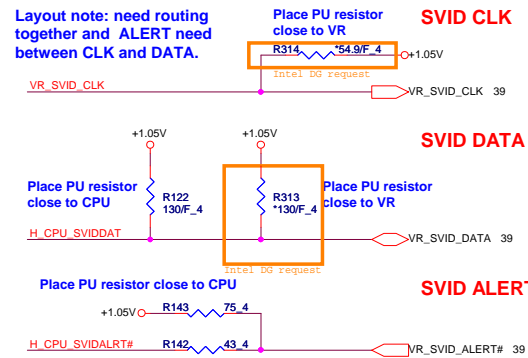
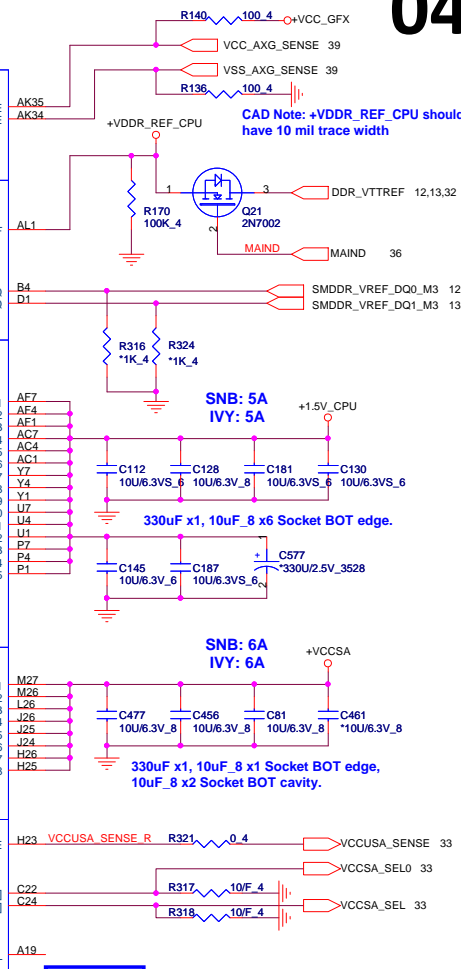
VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8

VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8

VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8

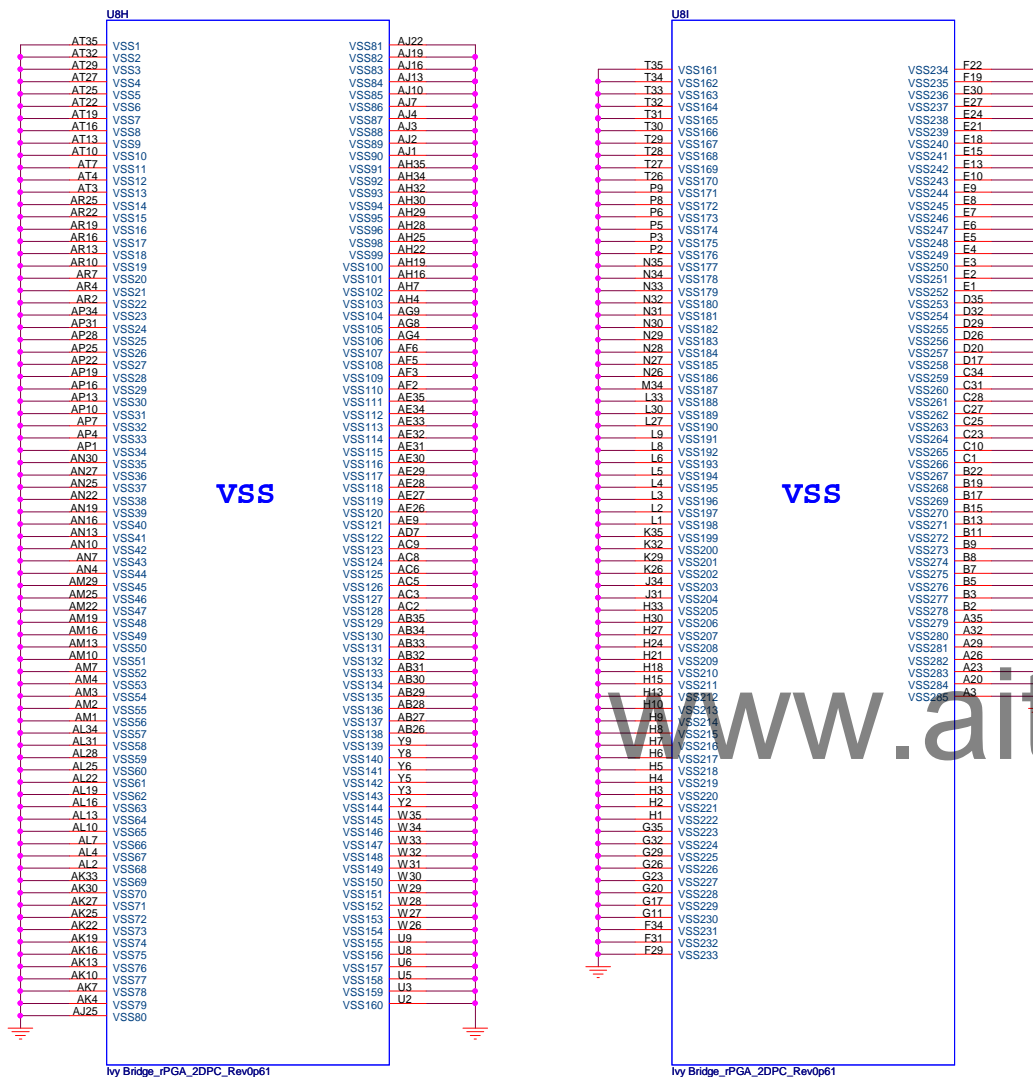
VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8

VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8





## Ivy Bridge Processor (GND)

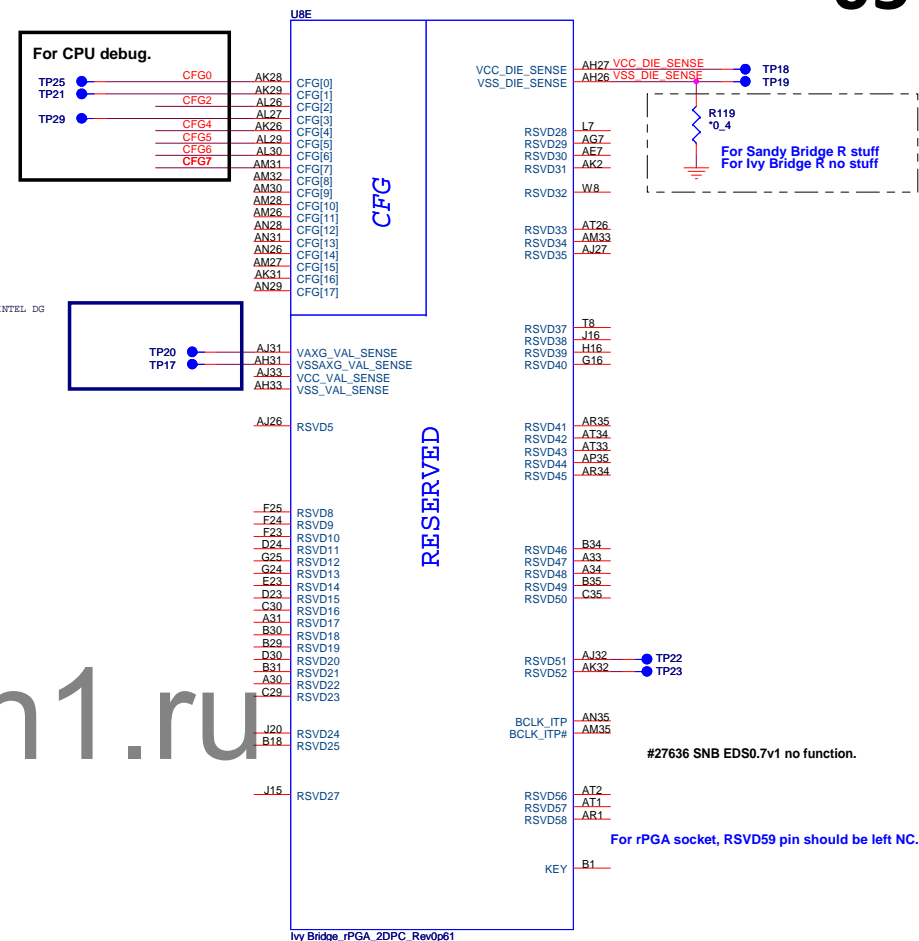


Ivy Bridge\_rPGA\_2DPC\_Rev0p61

Ivy Bridge\_rPGA\_2DPC\_Rev0p61

## Ivy Bridge Processor (RESERVED, CFG)

05

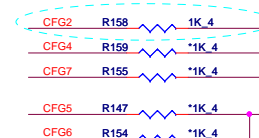


## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

(hh) TWH PEG bus is Lane Reversed



## CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PROJECT : TWC  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 4/4 (Ground)	A
Date: Monday, November 07, 2011	Sheet	5 of 40

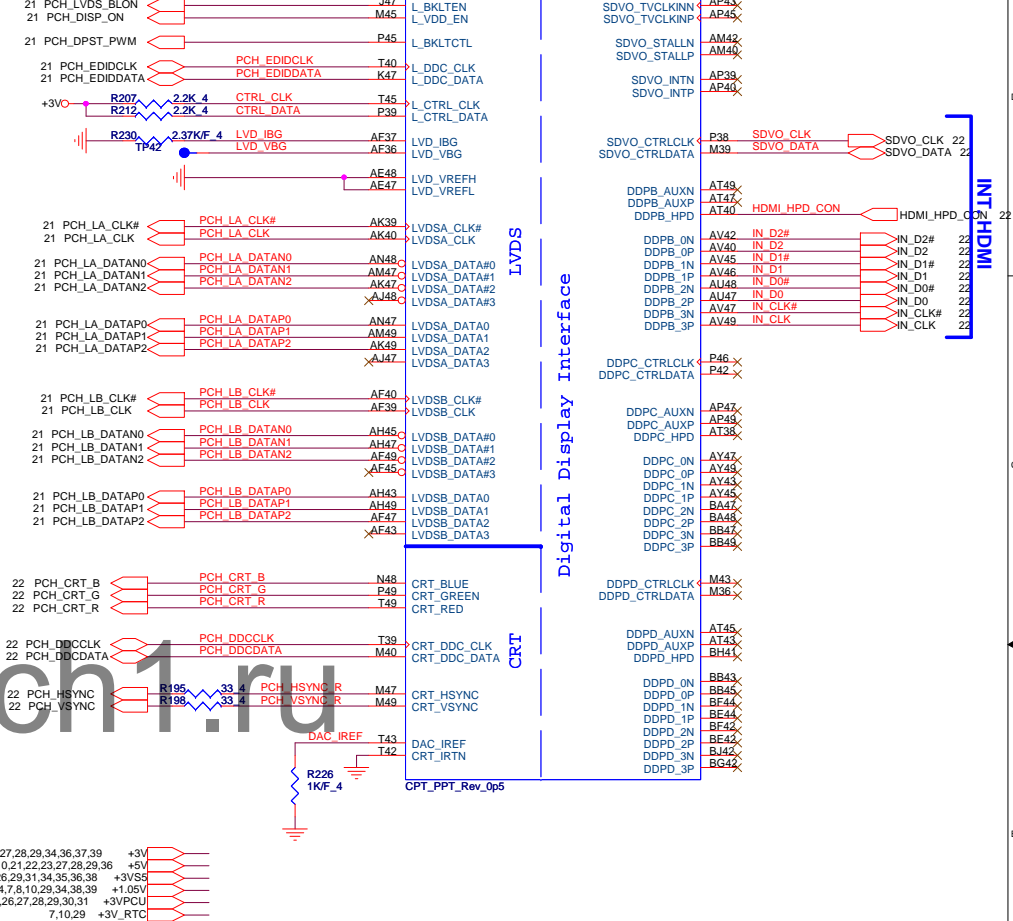
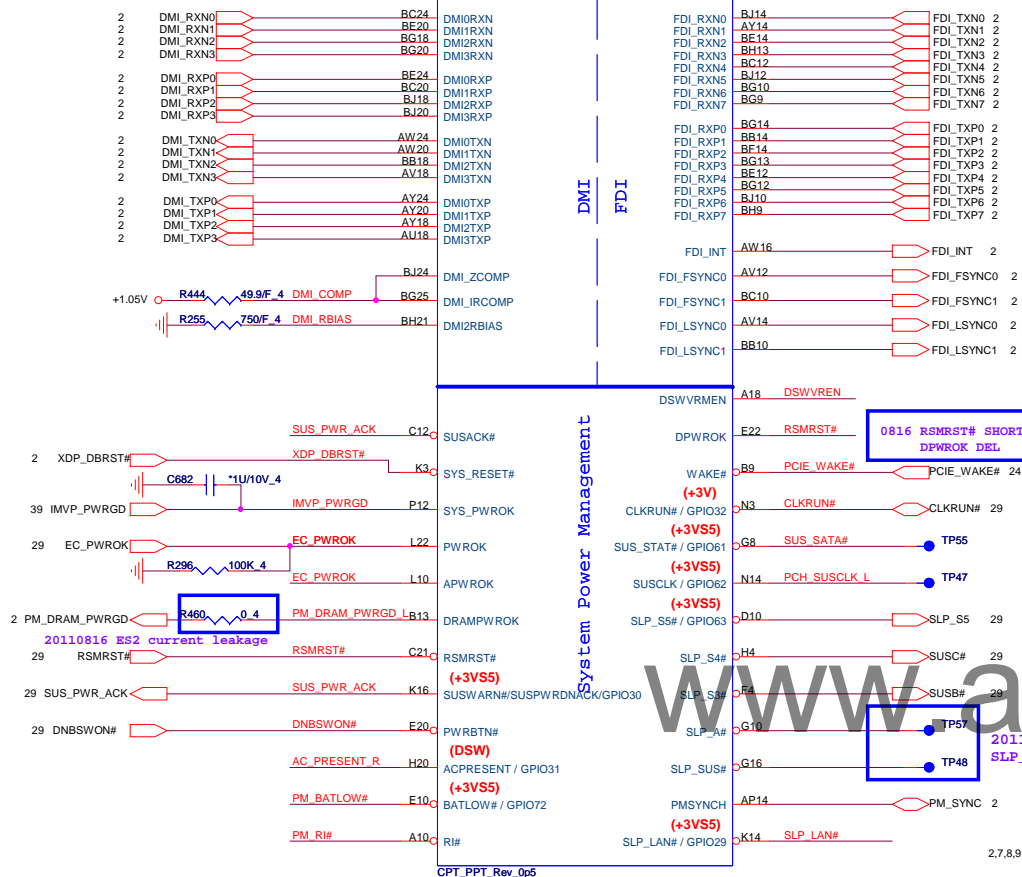
## Cougar Point/Panther Point (DMI,FDI,PM)

## Cougar Point/Panther Point (LVDS,DDI)

06

U13C

U13D



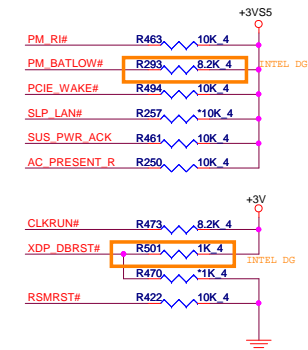
## PCH Pull-high/low(CLG)

## INT LVDS &amp; CRT disable (DIS only remove)

## INT HDMI disable (DIS only remove)

## System PWR\_OK(CLG)

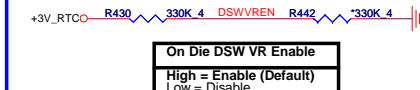
## DPWROK FOR DSW



PD Res place close to PCH

PCH to Res routing 50 ohm Impedance.  
Res to connector filter routing 37.5ohm Impedance.

EMI(near PCH)

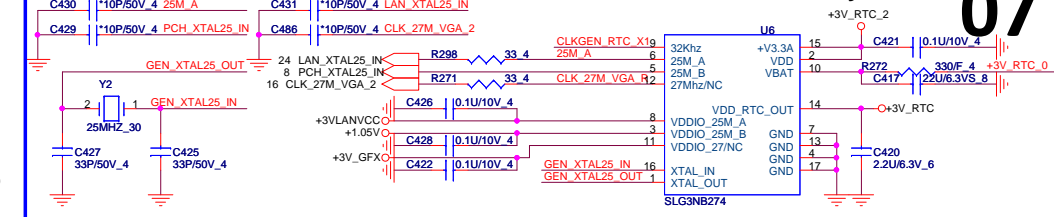
20110818 DEL  
INT HDMI Detect FunctionOn Die DSW VR Enable  
High = Enable (Default)  
Low = Disable

**PROJECT : TWC**  
**Quanta Computer Inc.**

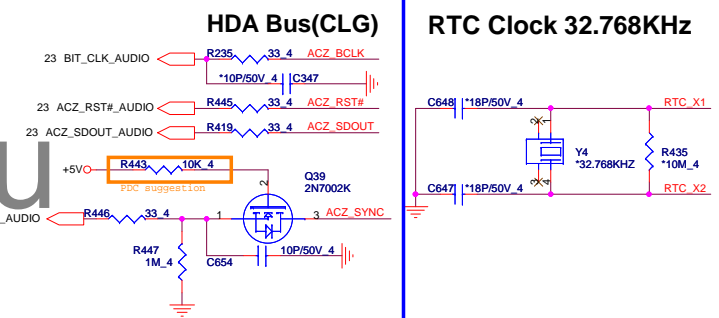
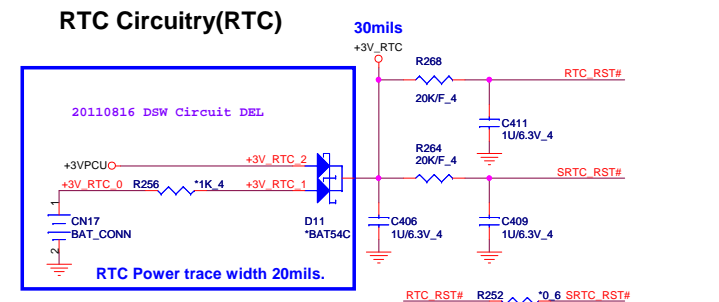
Size Custom Document Number PCH 1/6 (Host/Display) Rev A

Date: Monday, November 07, 2011 Sheet 6 of 40

## 07

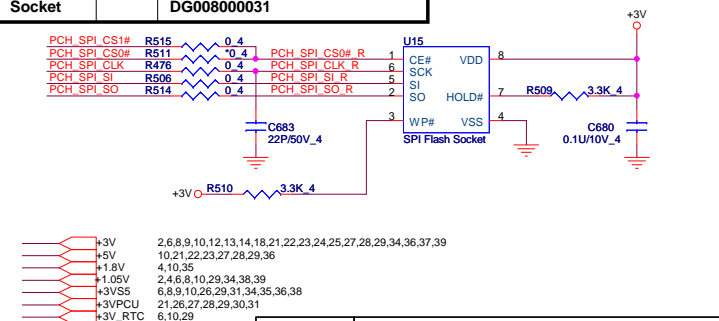


ODD (SATA1 6Gb/s)

**MINISATA (SATA1 1.5Gb/s)**

### PCH SPI ROM(CLG)

Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031



**PROJECT : TWC**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>PCH 2/6 (HDA/RTC/SATA/SPI)</b>	Rev A
Date: Tuesday, November 08, 2011	Sheet 7 of 40	

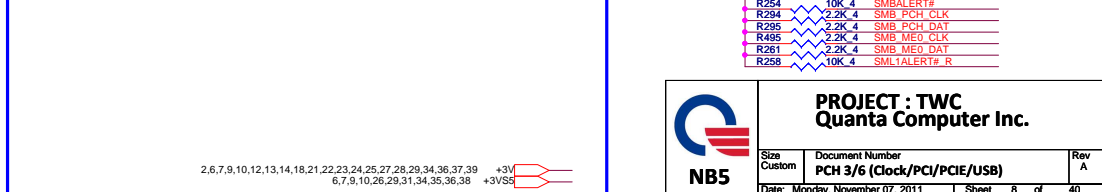
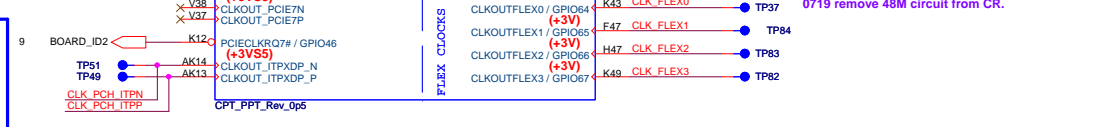
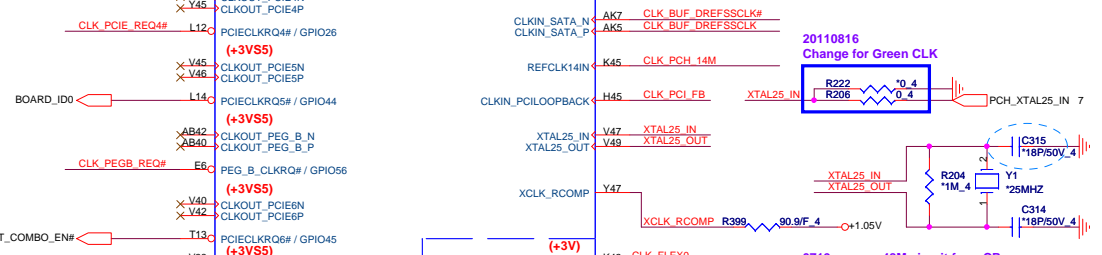
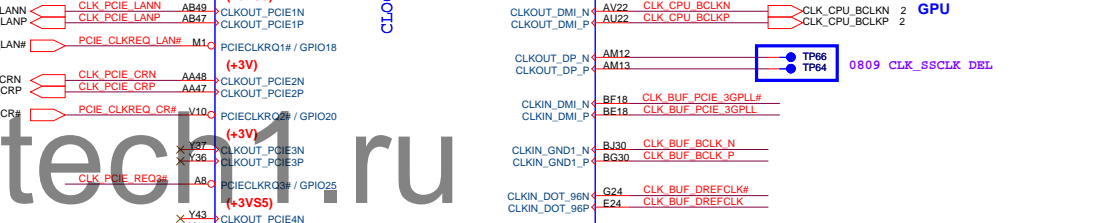
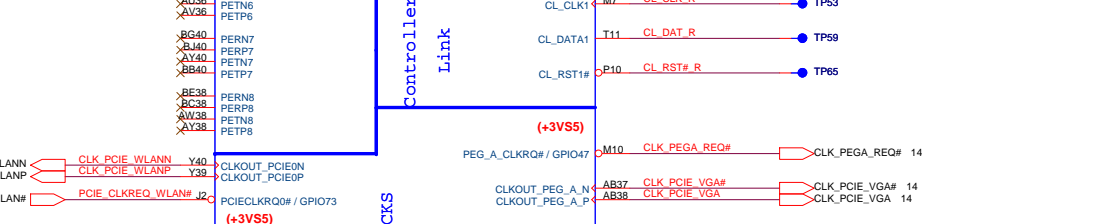
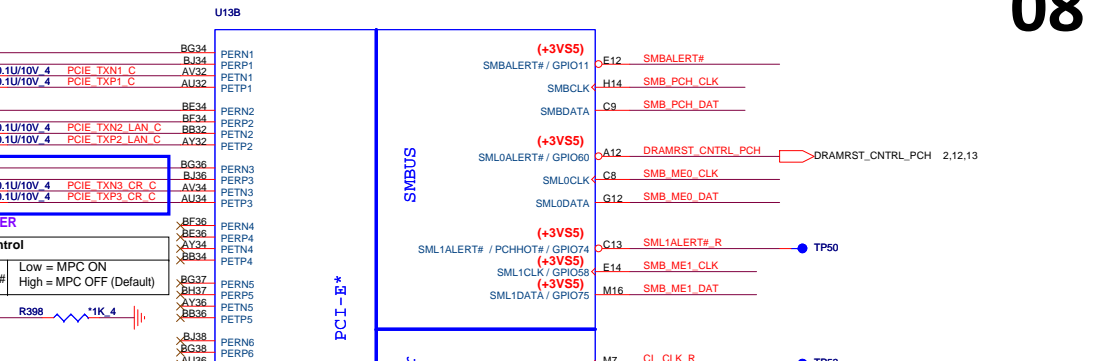
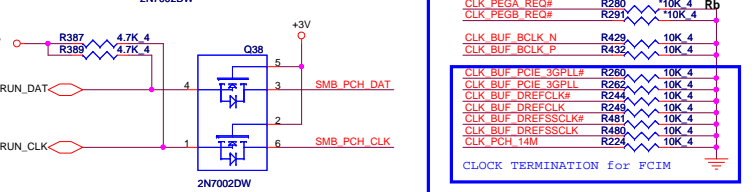
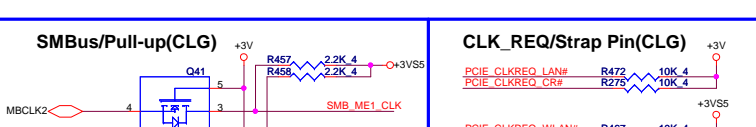
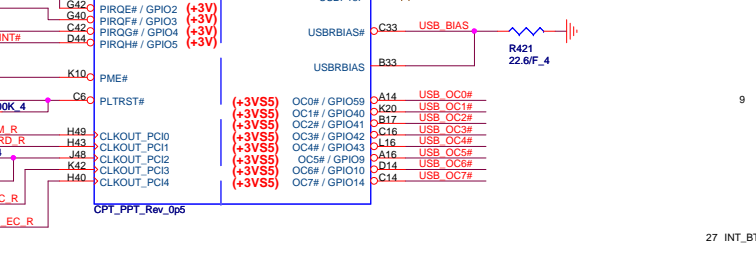
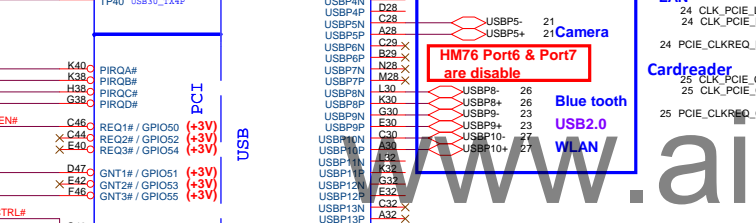
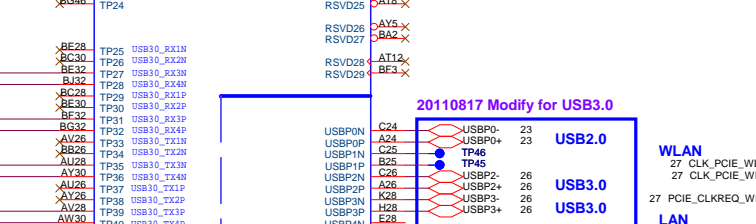
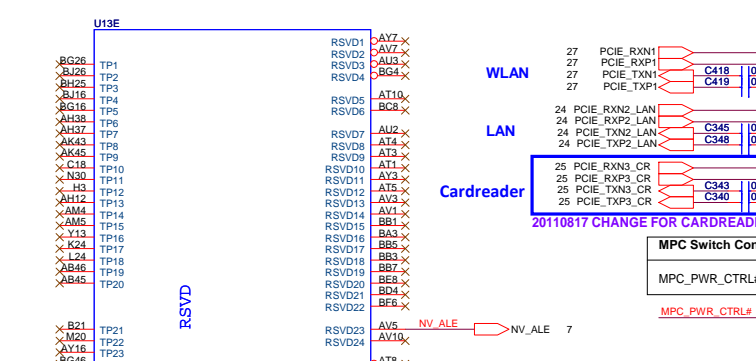
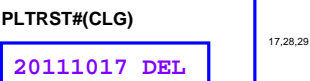
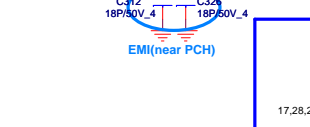
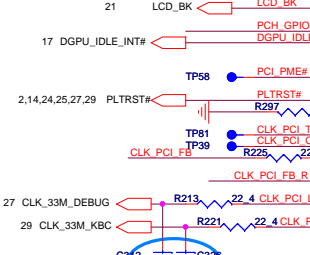
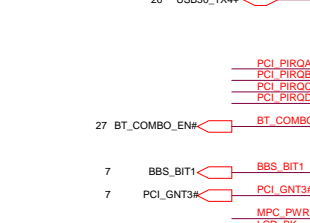
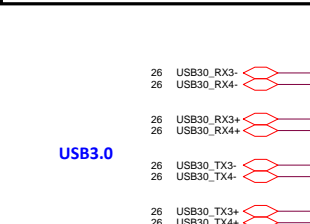
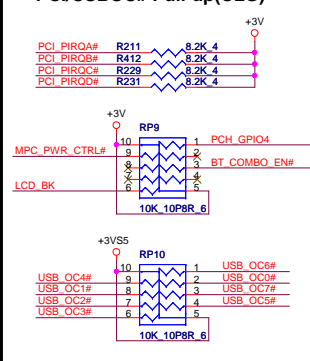
### PCH Strap Table

On Strap Table

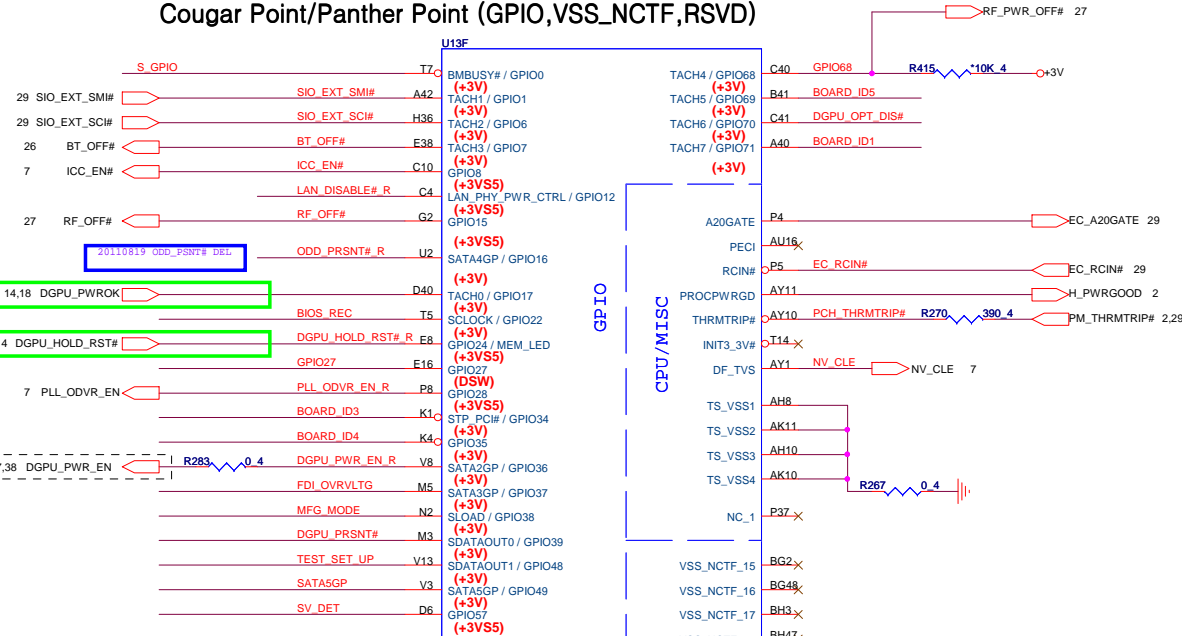
Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR <div>Different from Calpella</div>	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	0	LPC	<div>[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#</div>
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	0	LPC											
GPIO19 <div>Different from Calpella</div>	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 <div>Different from Calpella</div>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

## PC/USBOC# Pull-up(CLG)



### Cougar Point/Panther Point (GPIO,VSS\_NCTF,RSVD)



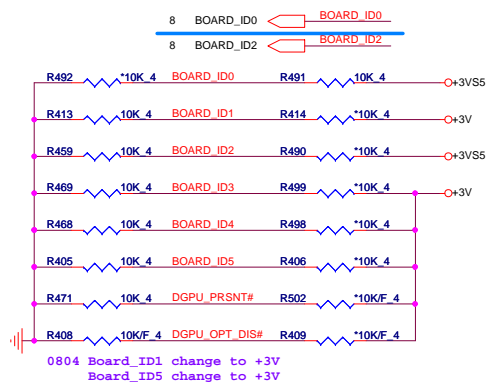
OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

BOARD_ID[3:0]	Model Name
0000	SW6C
0001	TWC
0010	JW2
0011	TBD
0100	TBD
0101	TBD
0110	TBD
0111	TBD
1000	TBD

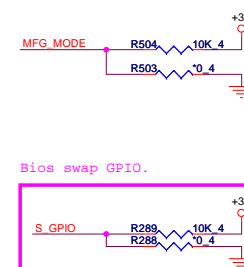
## Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	No Dolby=0, Dolby=1
BOARD_ID5	GPIO69	Reserve and pull low
DGPU_PRSTNS#	GPIO39	Reserve and pull low
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

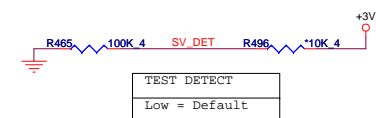
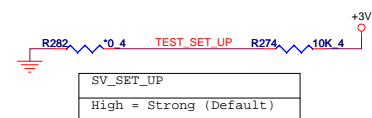
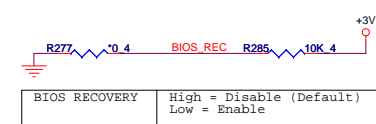
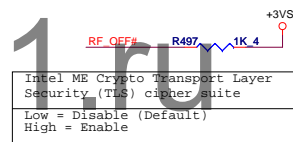
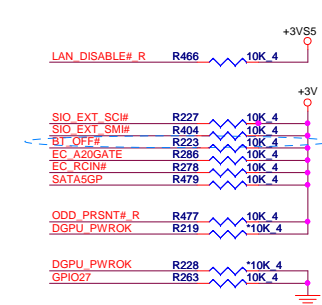
20110816 Define BRD\_ID[3:0]



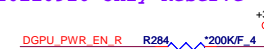
## MFG-TEST



### **GPIO Pull-up/Pull-down(CLG)**

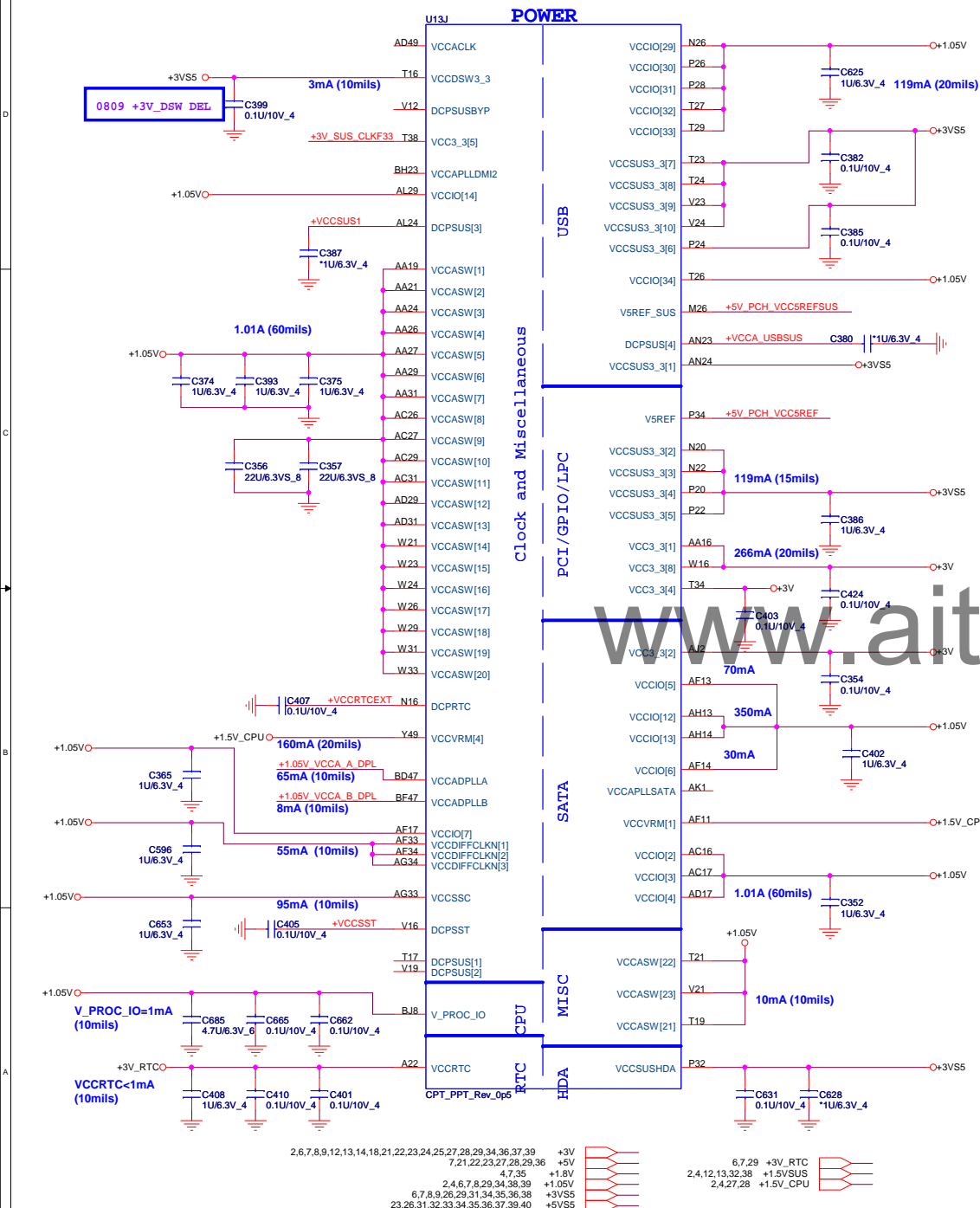


## 20110926 Only Reserve

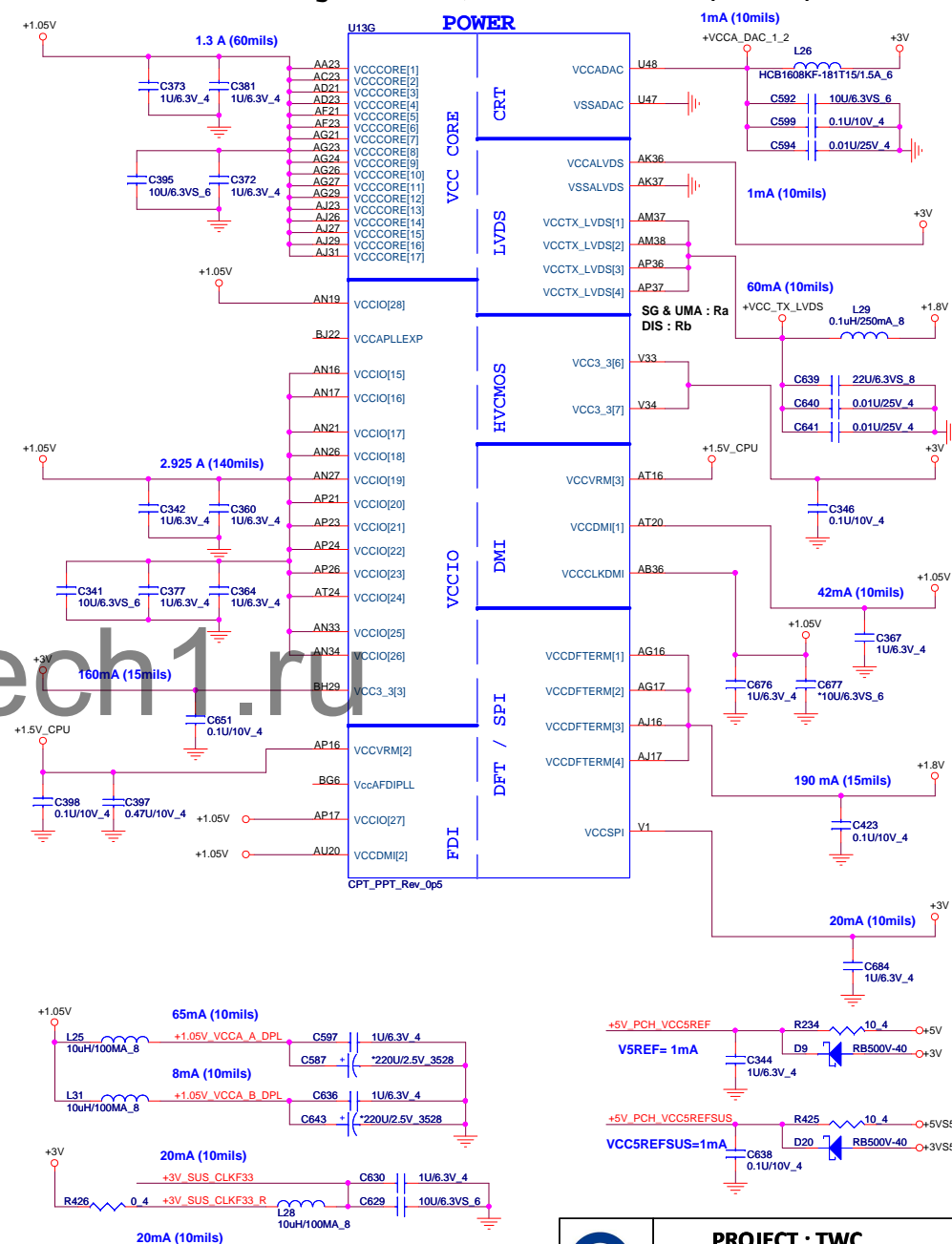


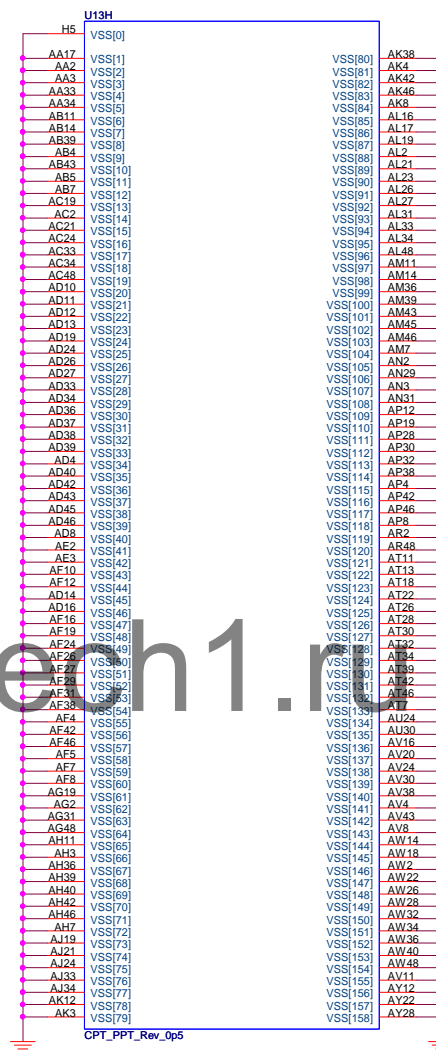


Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (POWER)

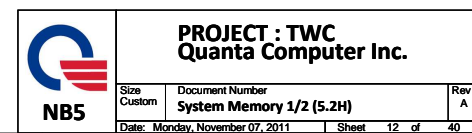




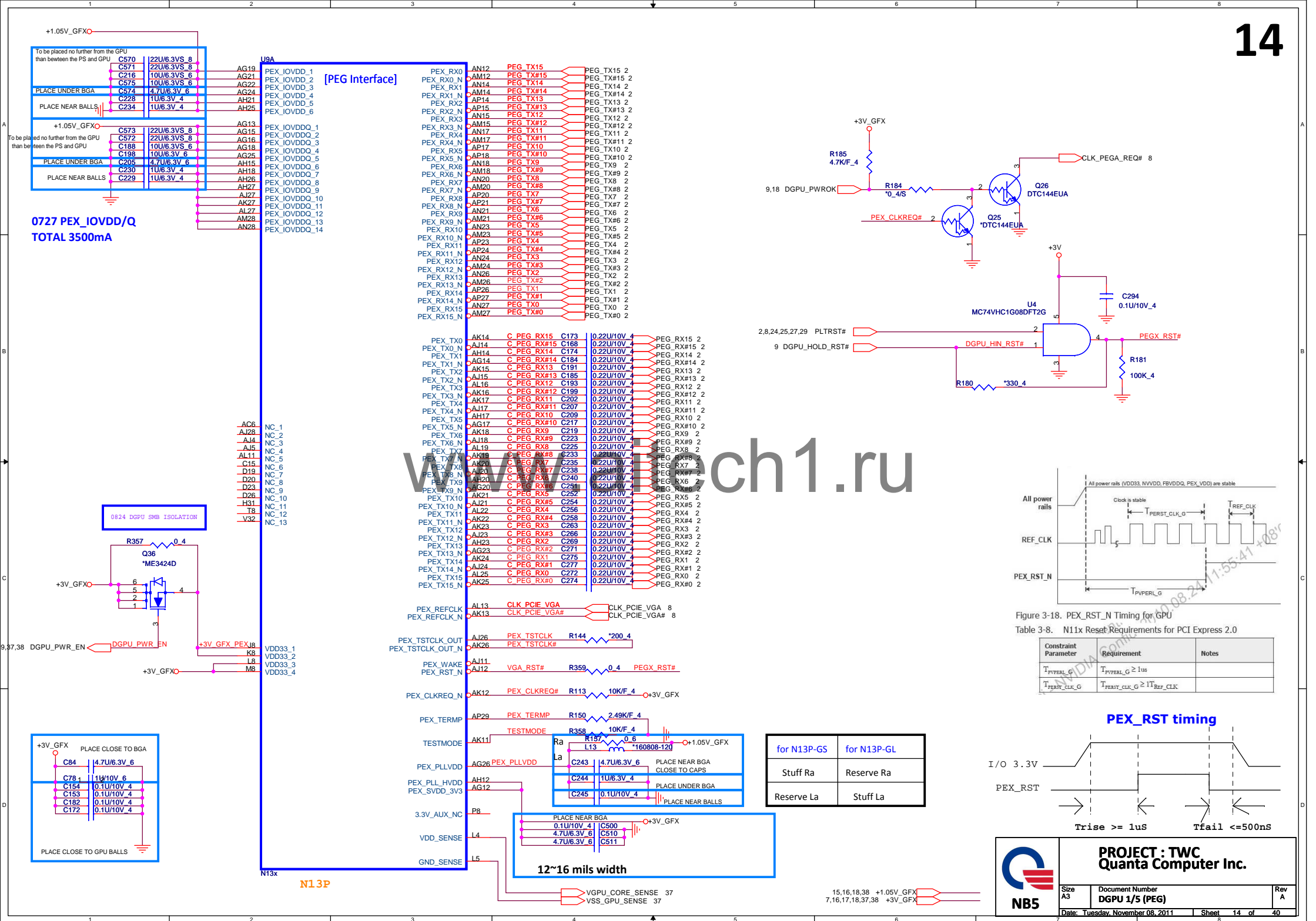


The schematic diagram illustrates the power plane layout for the DDR3 memory module, showing four main power planes and their associated components:

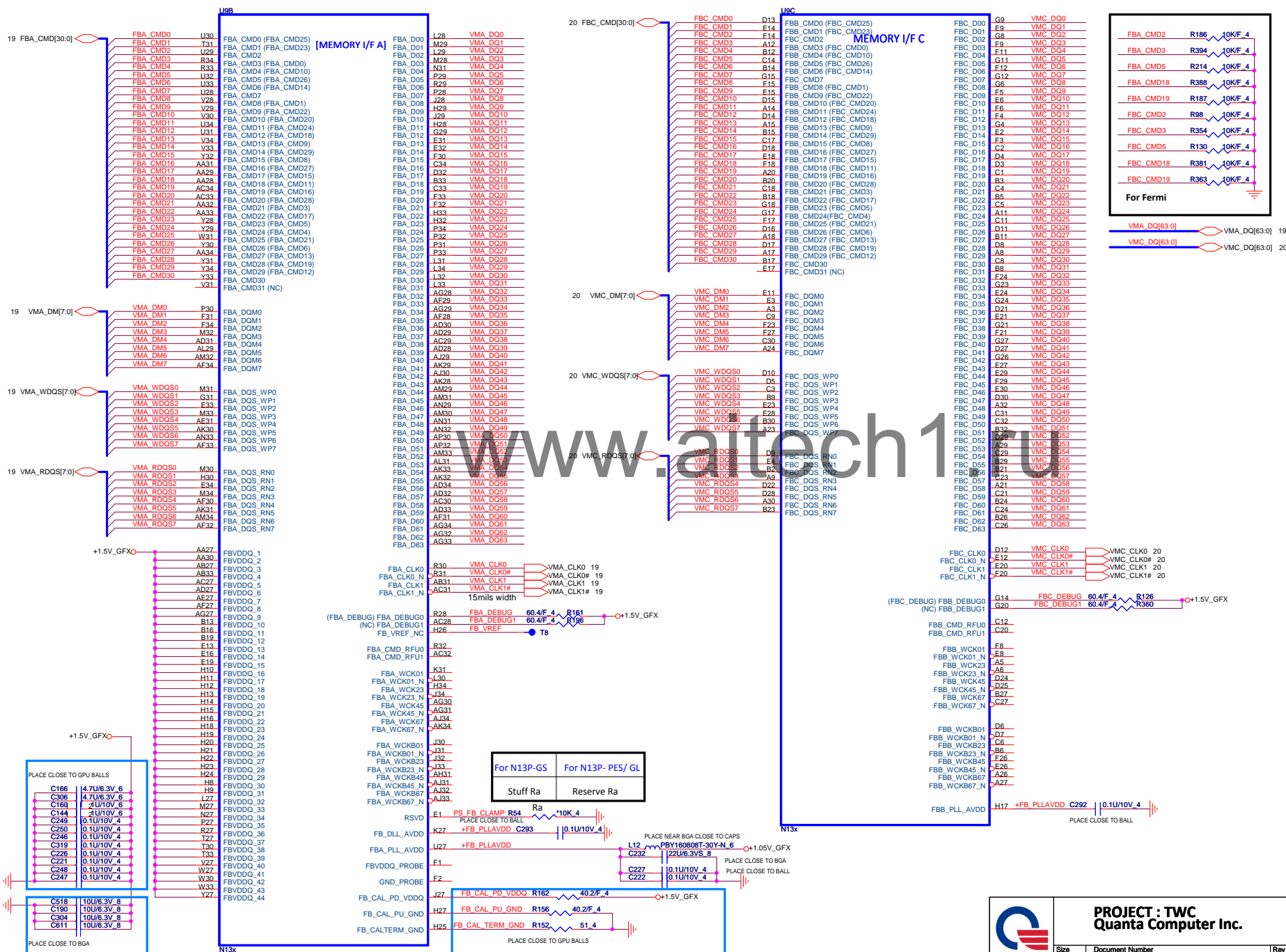
- +1.5VSUS:** This plane is connected to a 1.5V source and includes capacitors C107, C143, C148, C139, C32, C113, C99, C106, C52, C103, C120, C114, and C122. The capacitors are connected to ground.
- +0.75V\_DDR\_VTT:** This plane is connected to a 0.75V source and includes capacitors C287, C281, C286, C285, C288, and C289. The capacitors are connected to ground.
- +SMDDR\_VREF\_DIMM:** This plane is connected to a 0.75V source and includes capacitors C152 and C140. The capacitors are connected to ground.
- +SMDDR\_VREF\_DQ0:** This plane is connected to a 0.75V source and includes capacitors C34 and C29. The capacitors are connected to ground.
- +3V:** This plane is connected to a 3V source and includes capacitors C276 and C268. The capacitors are connected to ground.







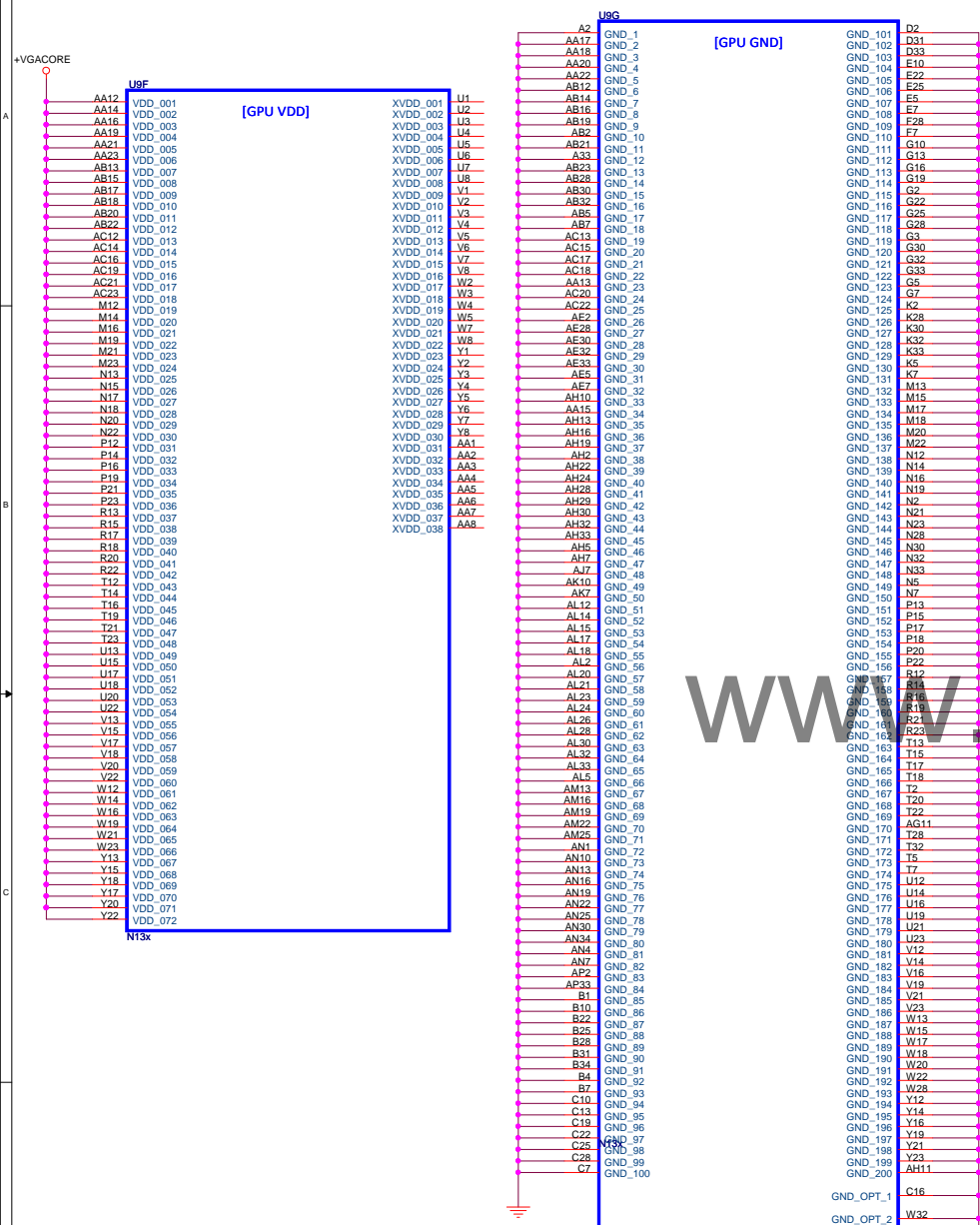




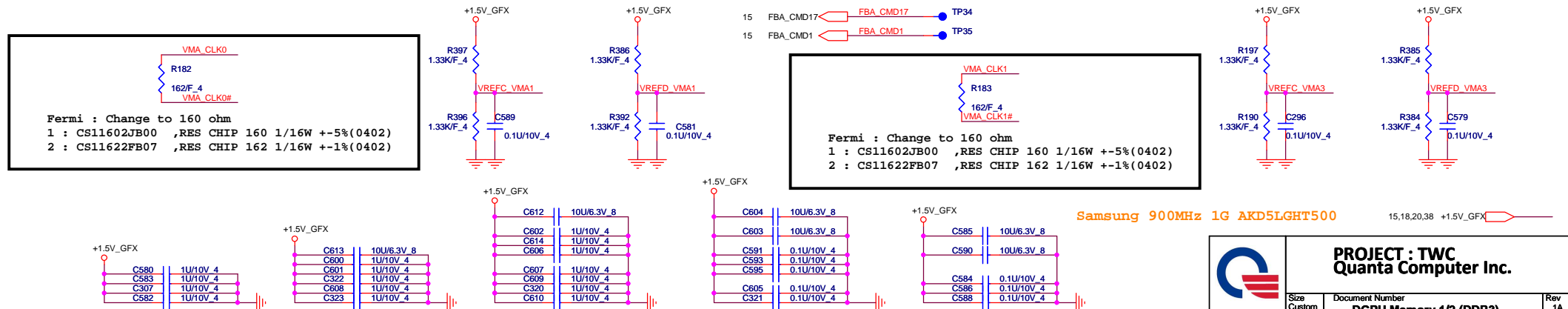
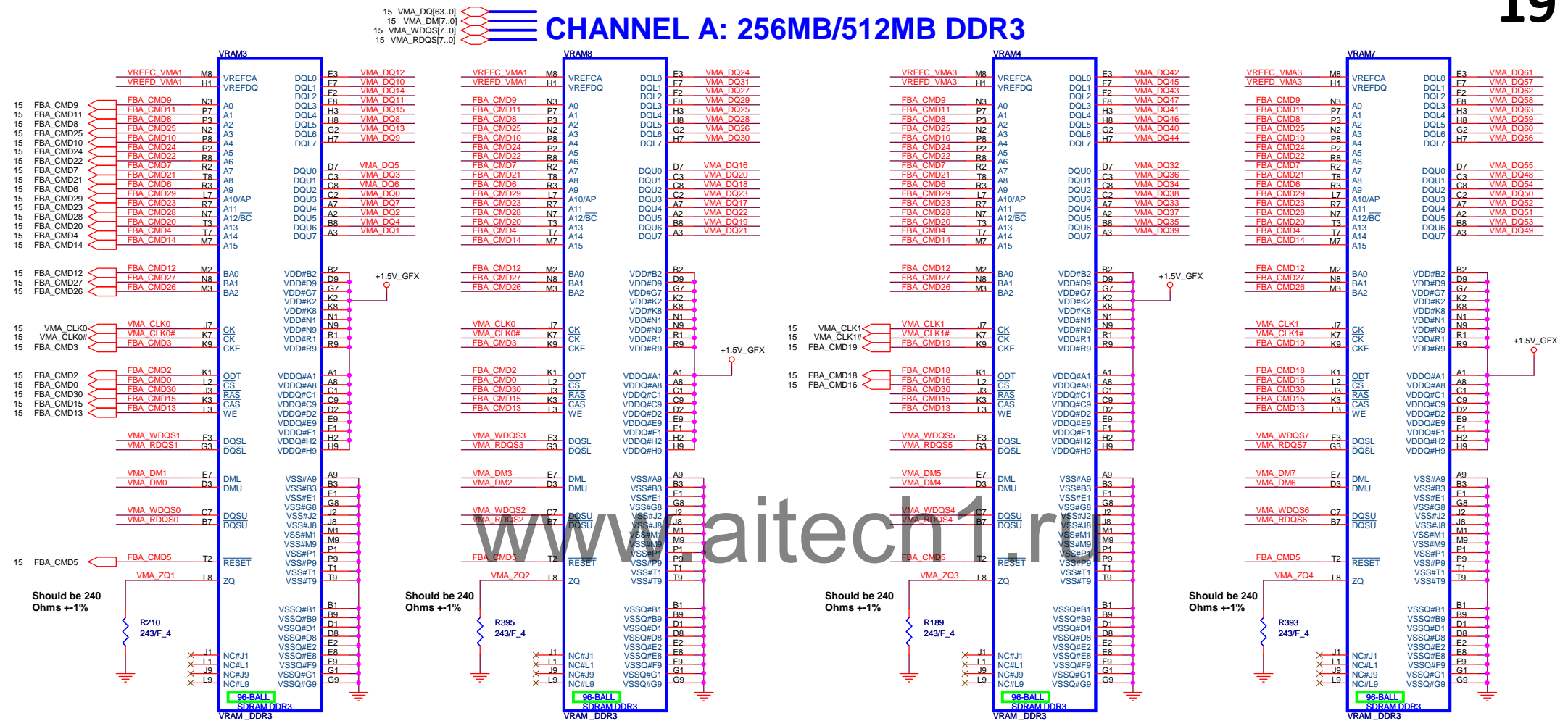


Size A3	Document Number <b>DGPU 3/5 (Display)</b>	Rev A
Date: Tuesday, November 08, 2011	Sheet 16 of 40	



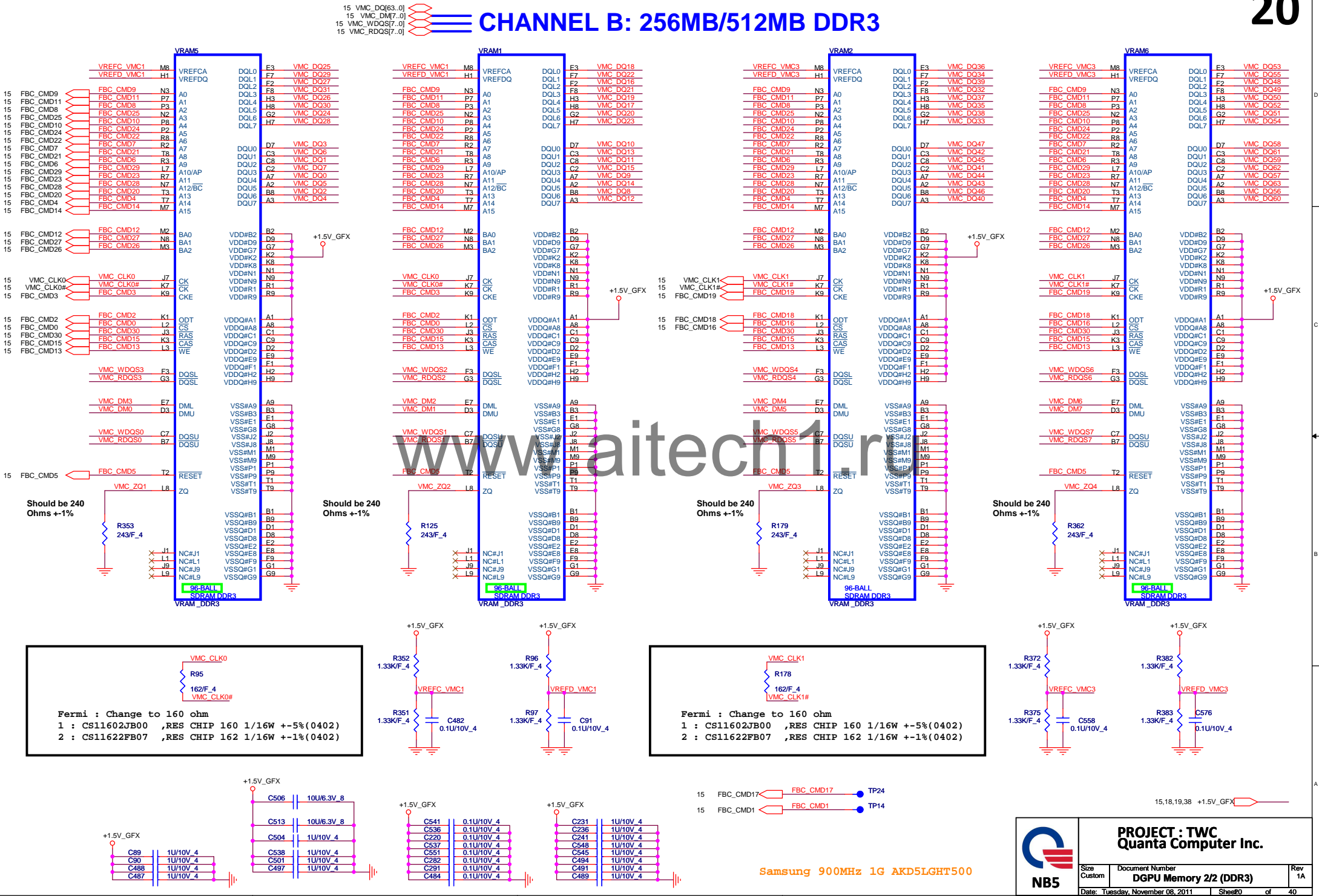


**CHANNEL A: 256MB/512MB DDR3**

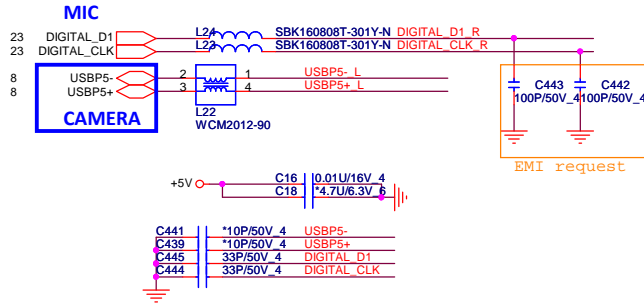




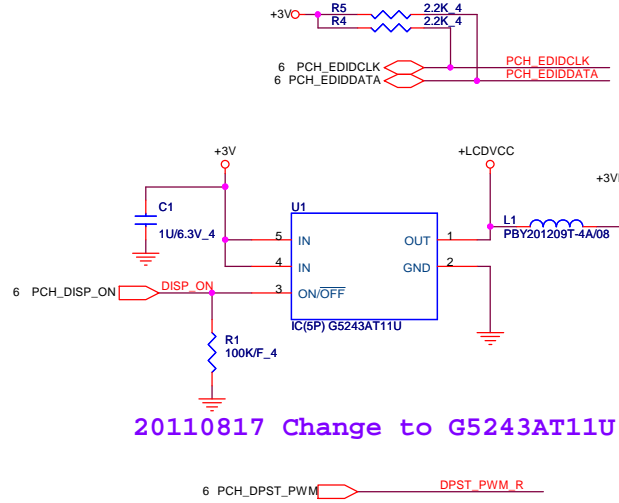
**CHANNEL B: 256MB/512MB DDR3**



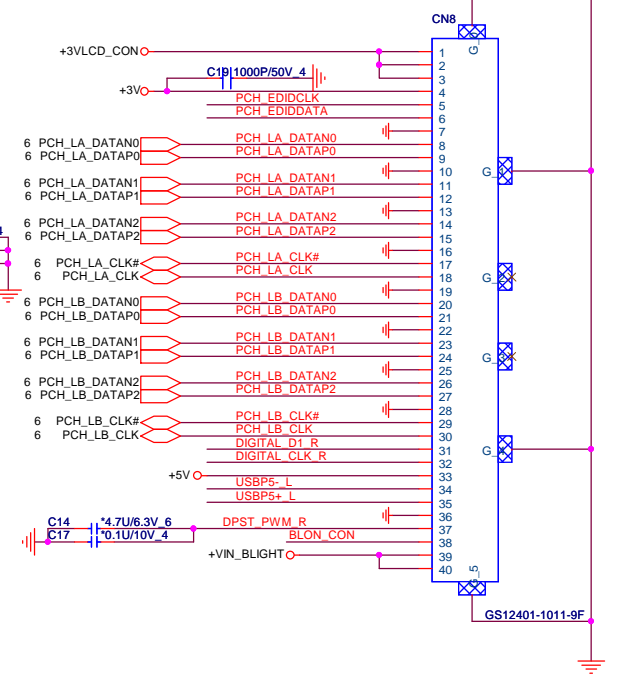
### USB Camera Connector



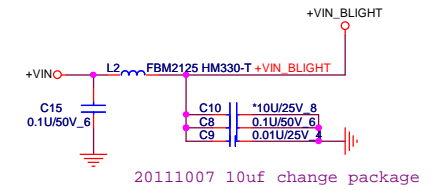
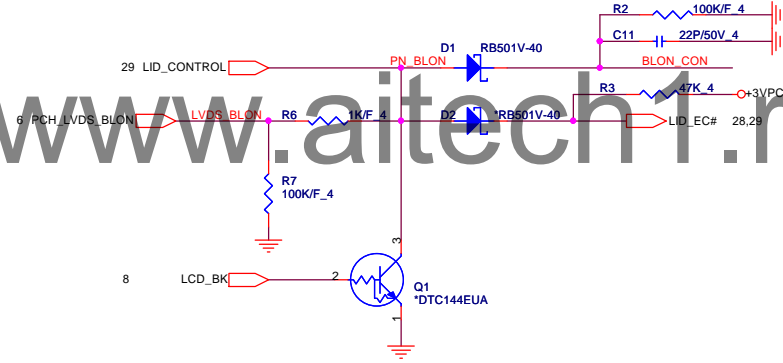
20110817 CAMERA REGULATOR DEL



20110817 Change to G5243AT11U




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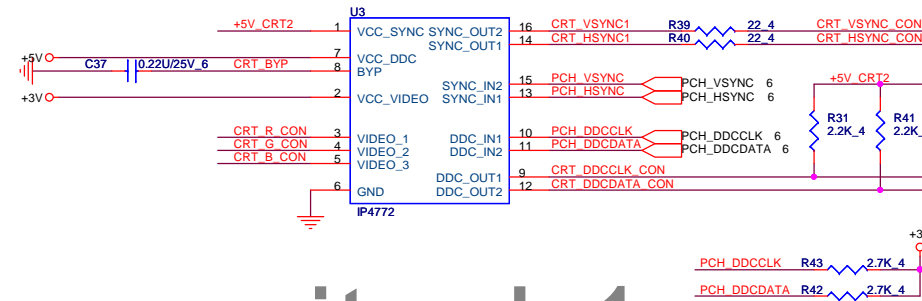
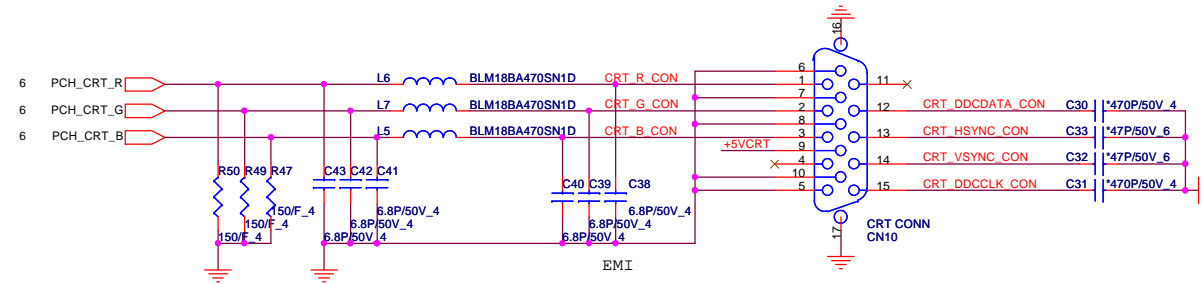
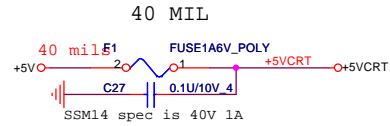


20111007 10uf change package

2,6,7,8,9,10,12,13,14,18,22,23,24,25,27,28,29,34,36,37,39	+3V
7,26,27,28,29,30,31	+3VPCU
7,10,22,23,27,28,29,36	+5V
30,31,32,34,36,37,38,40	+VIN
36,38	+12VALW
10,23,26,31,32,33,34,35,36,37,39,40	+5VSS

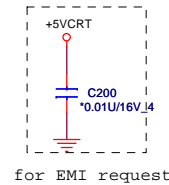
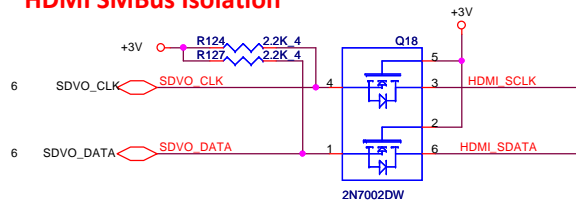
 <b>NB5</b>	<b>PROJECT : TWC</b>				Rev A
	<b>Quanta Computer Inc.</b>				
	Size Custom	Document Number <b>LCD Connector (LVDS)</b>			
Date: Tuesday, November 08, 2011		Sheet 21 of 40			

## CRT PORT



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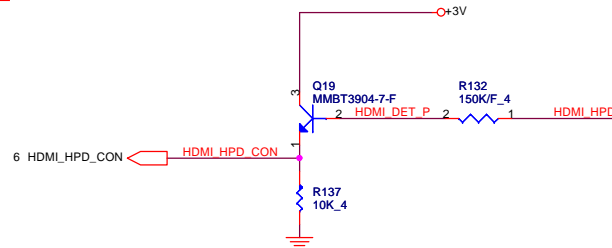
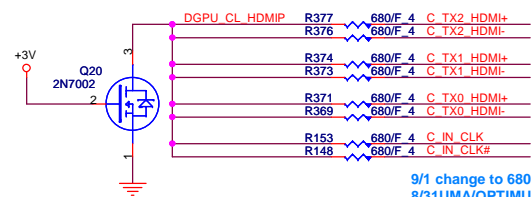
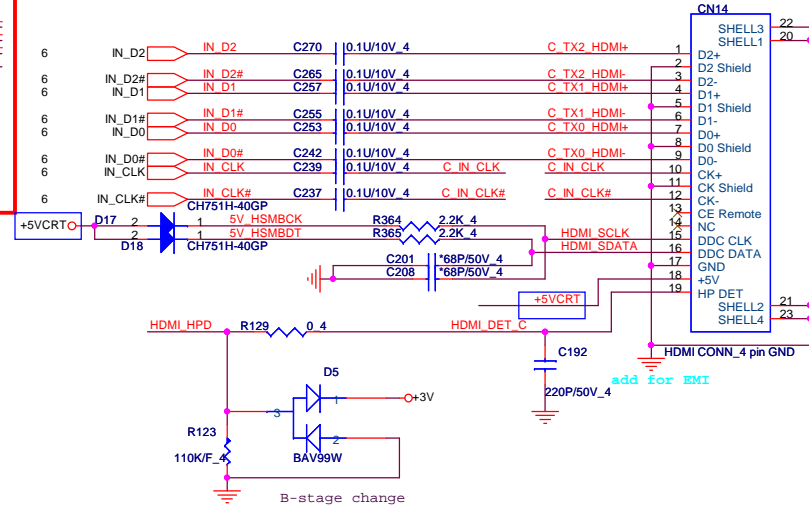
## HDMI SMBus Isolation



## EMI Solution

C TX2 HDMI+	R172	*130F_4	C TX2 HDMI-
C TX1 HDMI+	R166	*130F_4	C TX1 HDMI-
C TX0 HDMI+	R160	*130F_4	C TX0 HDMI-
C IN_CLK	R151	*130F_4	C IN_CLK#

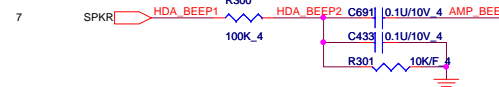
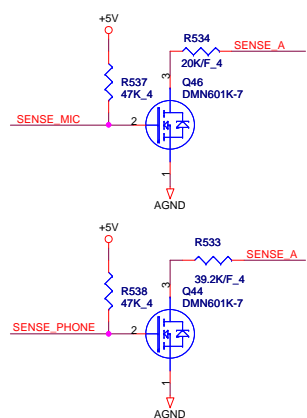
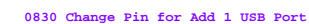
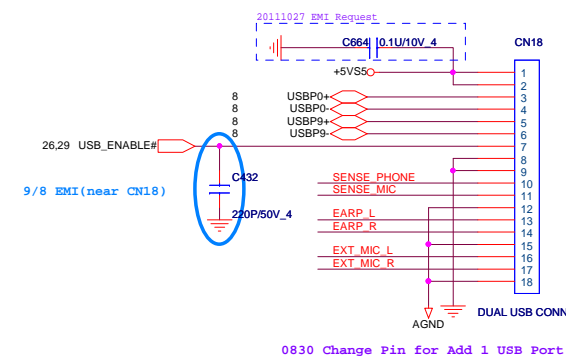
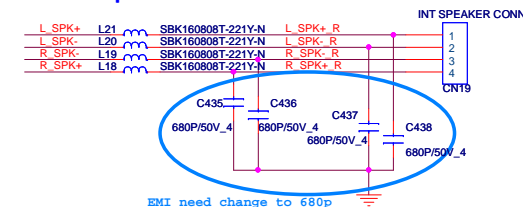
## HDMI PORT

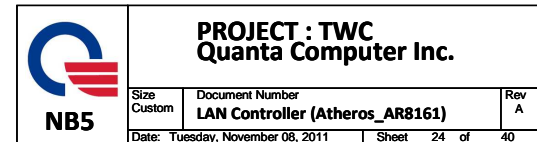


PROJECT : TWC  
Quanta Computer Inc.

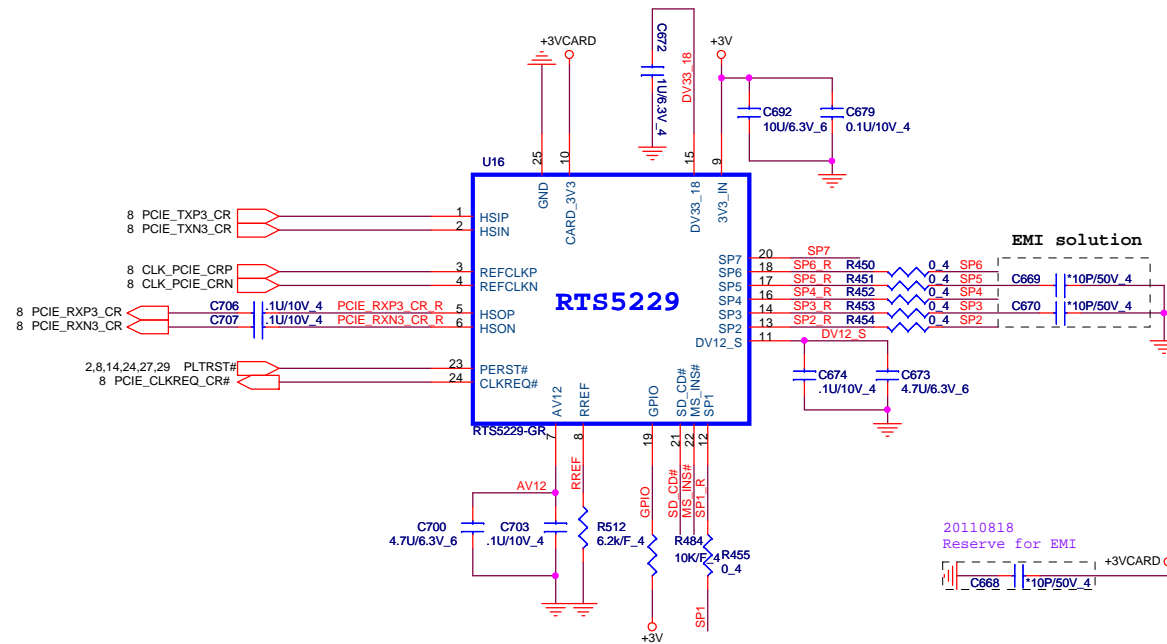
Size	Document Number	Rev
Custom	CRT/HDMI Connector	A
Date: Tuesday, November 08, 2011	Sheet 22 of 40	

9/1 change to 680ohm  
8/31UMA/OPTIMUS-680 ohm, DISCRETE-499 ohm







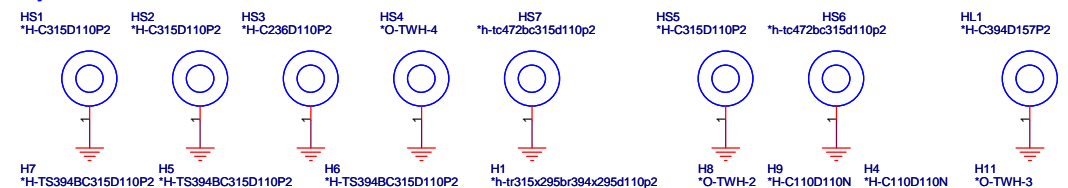


## Note:

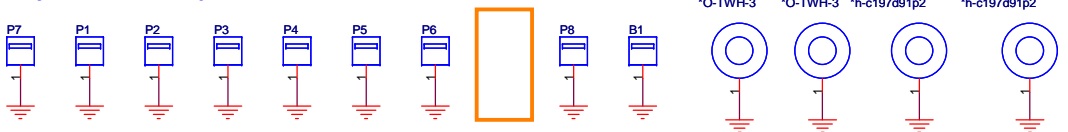
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

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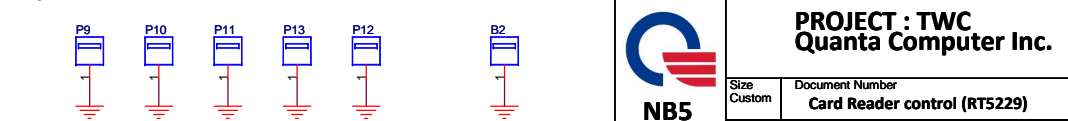
## System Screw Hold



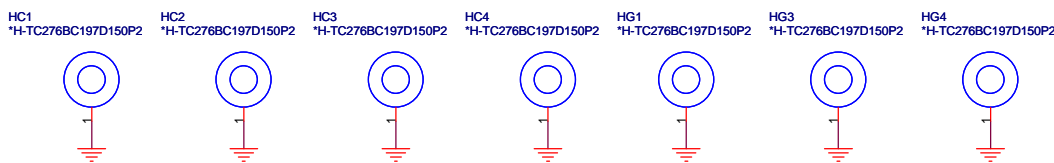
## System Pad(Top)



## System Pad(Button)

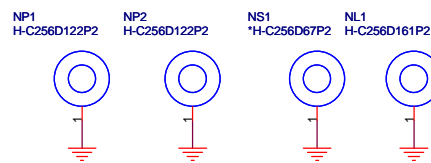


## CPU Bracket

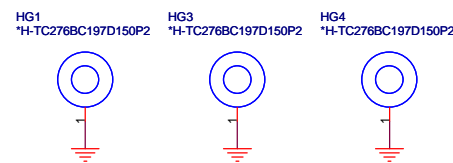


## MDC NU Screw Hold

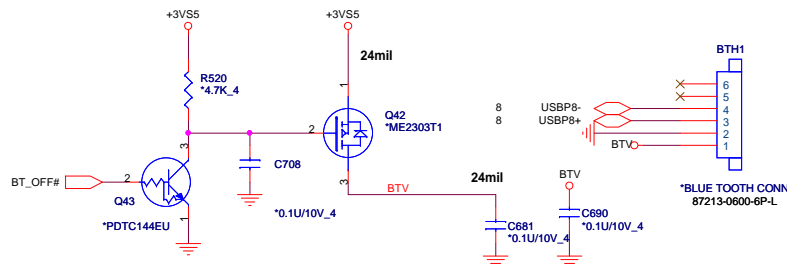
## PCH NU Screw Hold



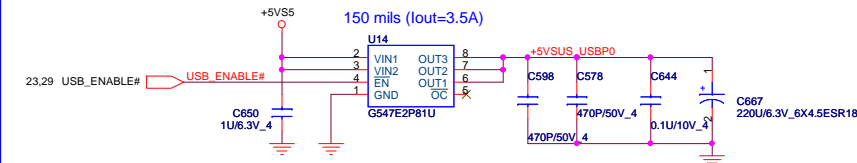
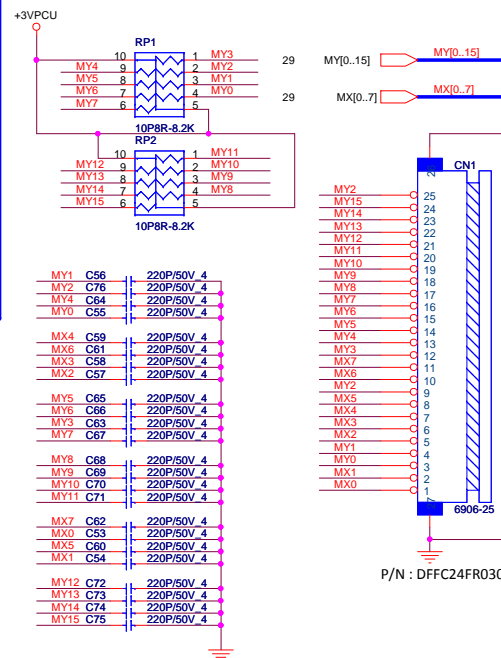
## GPU Bracket



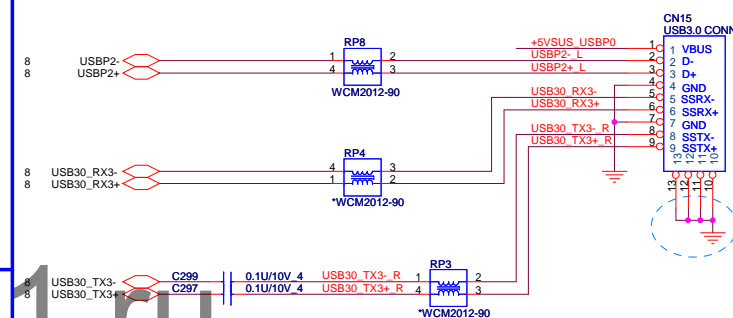
## BLUETOOTH



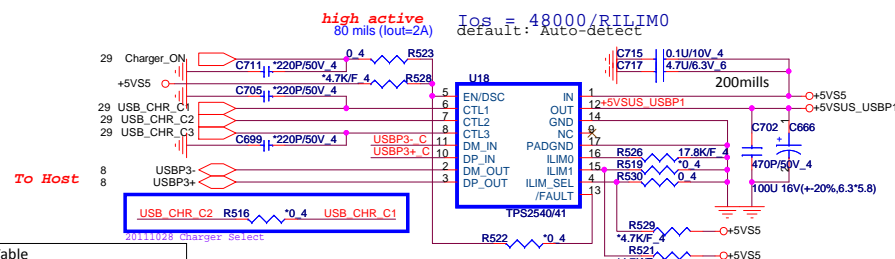
## Keyboard Connector



**USB3.0 X 2/USB2.0 COMBO**      **USB 3.0**



## Charger USB

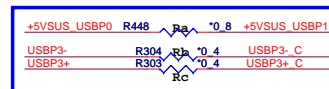


CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated charging port, auto-detect (DCP)
X	1	0	Standard downstream port, USB 2.0 Mode.(SDP)
1	1	1	Charging downstream port, BC1.2 (draft).(CDP)

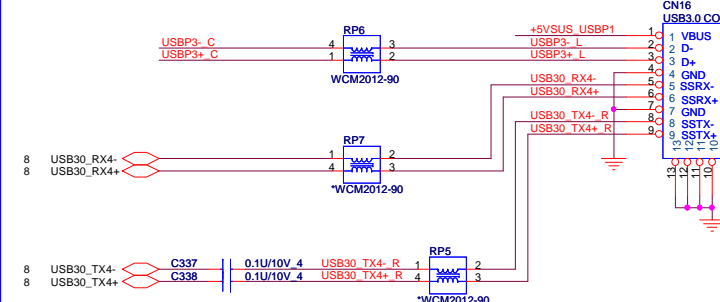
LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
change mode	CDP	CDP	DCP	DCP
user define and wake up		SDP		OFF

U18	Ra	Rb	Rc
stuff	unstuff	unstuff	unstuff
unstuff	stuff	stuff	stuff

20111011 modify:  
Add R448, R304, R303 for reserve TPS2543.



## USB 3.0

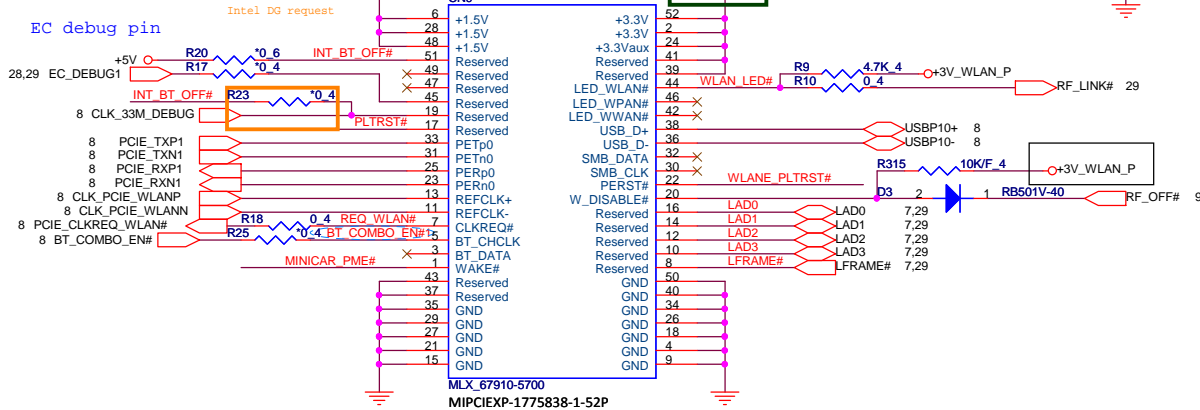


**PROJECT : TWC**  
**Quanta Computer Inc.**

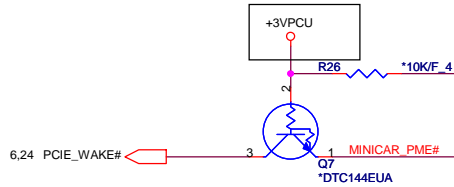
Size Custom	Document Number <b>USB 3.0/KEY Connector</b>	Rev.
Date: Monday, November 07, 2011	Sheet 26 of 38	

## Mini Card WLAN/BT(Optional)

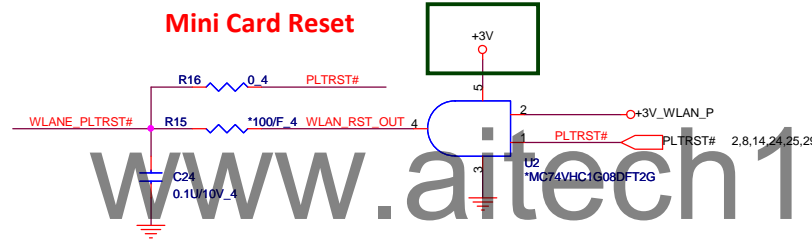
EC debug pin



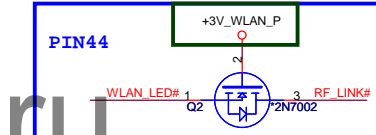
## Support Wake Function(Reserve)



## Mini Card Reset



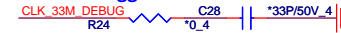
## Avoid leakage issue



## 1GE mini-pcie power status

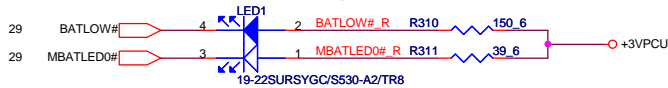
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

## For EMI Suggestion



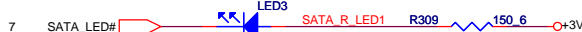
## LED Status

(Orange)

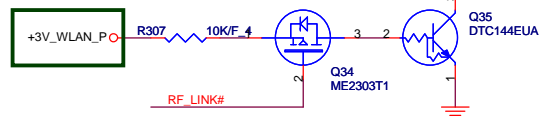


(White)

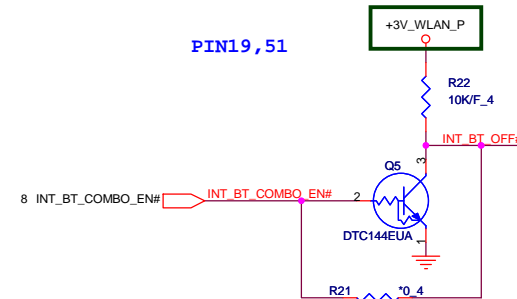
(White)



(White)

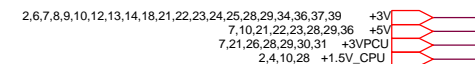


PIN19, 51



## 9/4 Intel COMBO card control circuit

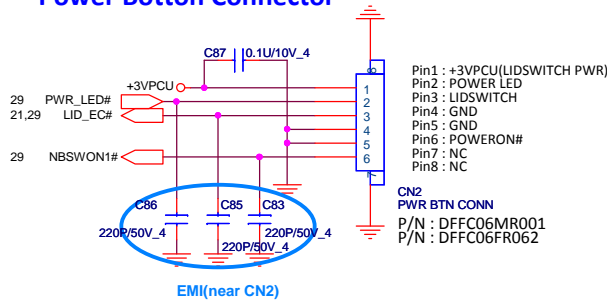
- 1.add R1001,R1002,Q1001
- 2.add net name"INT\_BT\_COMBO\_EN#" -> "INT\_BT\_OFF#"



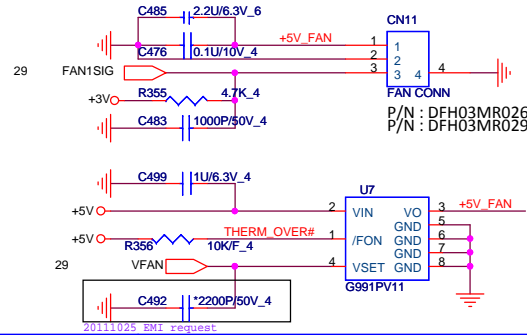
**PROJECT : TWC**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	Audio Codec (Realtek_ALC269)	A
Date: Monday, November 07, 2011		Sheet 27 of 40

## Power Button Connector

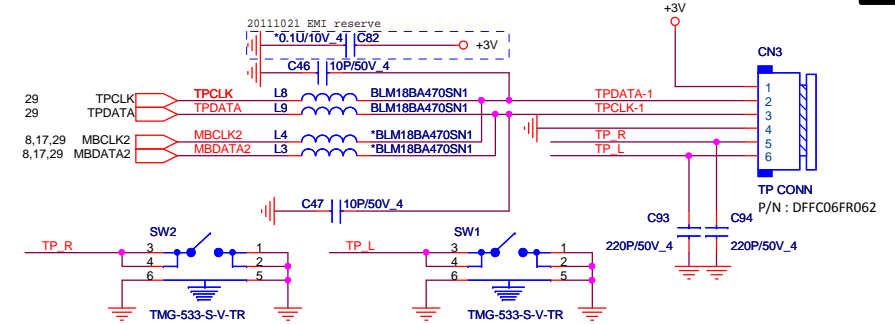


## CPU FAN

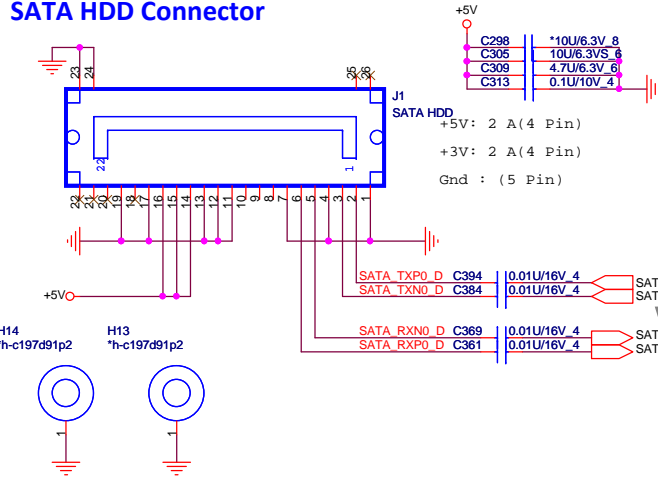


## Touch Pad Connector

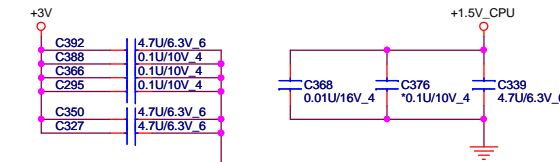
B-stage change footprint to 88513-0601-6p-l-smt



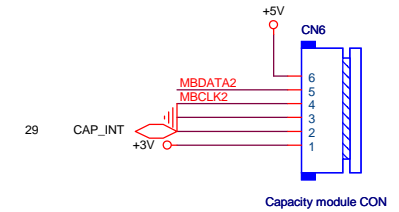
## SATA HDD Connector



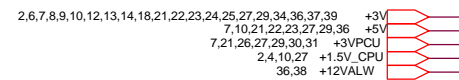
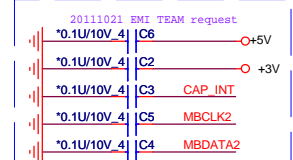
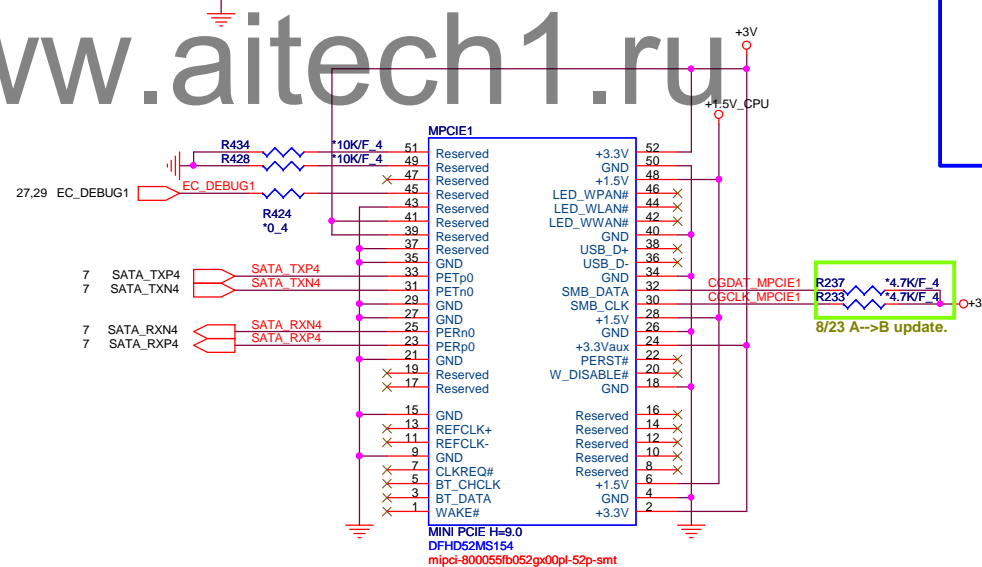
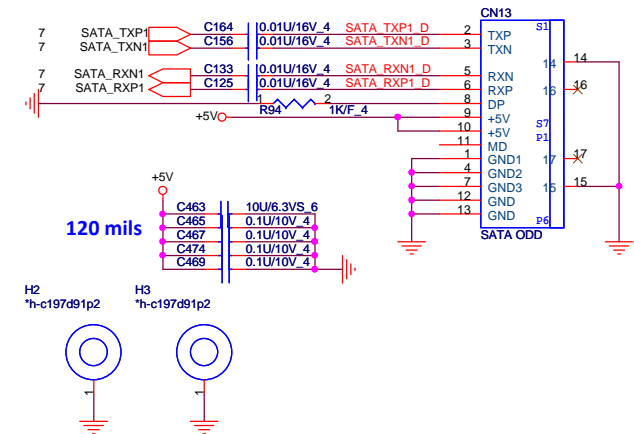
## Mini PCI-E Card 2- Full size MINISATA

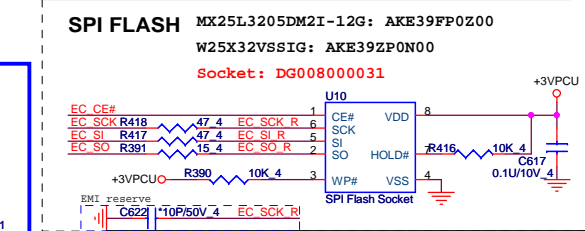
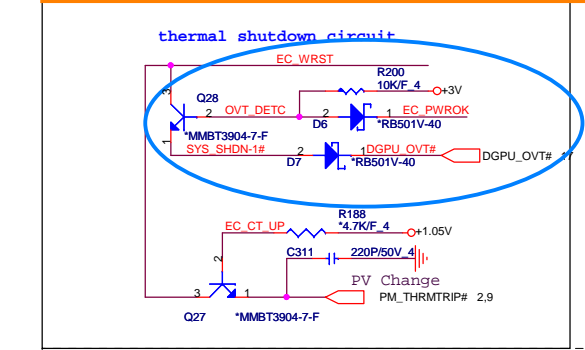
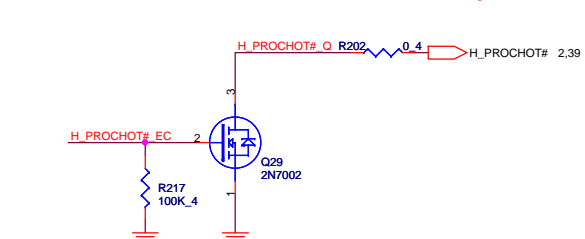


## Capacity Module connector

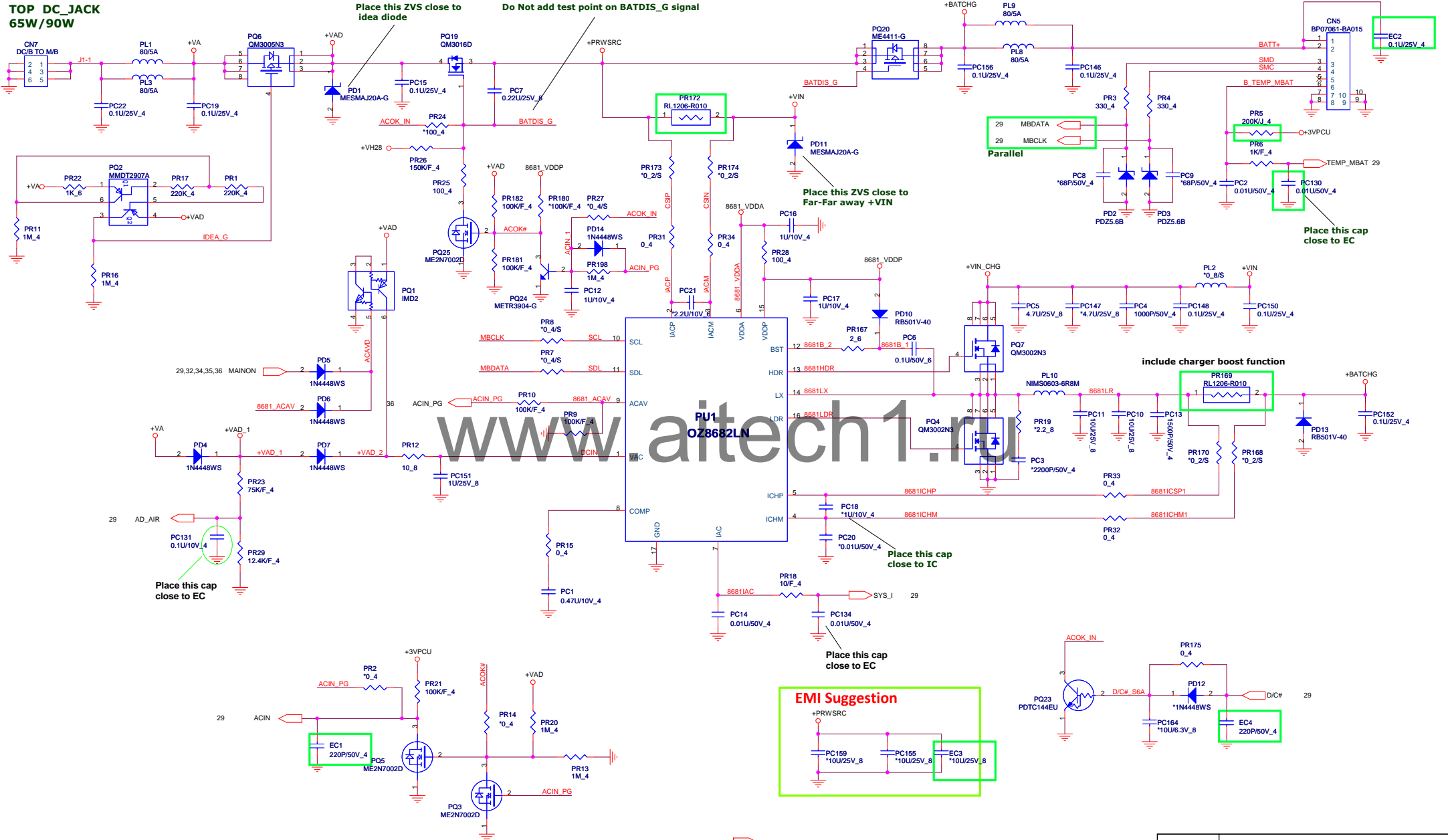


## SATA ODD Connector





**TOP DC\_JACK  
65W/90W**



21,31,32,34,36,37,38,40	+VIN	
36	+VAD	
36	+VH28	
36	+VAD_1	
7,21,26,27,28,29,31	+3VPCU	



+5V +/- 5%  
Continue current:4A  
Peak current:6A  
OCP minimum:7.5A

+3.3 Volt +/- 5%  
Continue current:4A  
Peak current:6A  
OCP minimum:7.5A

**Rds(on) 18m ohm**

**Rds(on) 18m ohm**

( VTT/2A )

+0.75V\_DDR\_VTT

PC136 10U/6.3V\_8  
PC133 10U/6.3V\_8

+1.5VSUS  
PC135 \*0.1U/50V\_6

8207BST  
PR267 2\_6  
8207BSTR

PC244 0.1U/25V\_4

$RILIM = ILIM \times RDS(ON) / 10\mu A$

PR269 6.98K/F\_4

8207CS

PC137 1U/6.3V\_4

PC138 1U/6.3V\_4

PR160 0\_4

HWPG 29,31,33,34,35

PR164 10K/F\_4

PR165 10K/F\_4

PC140 0.1U/10V\_4

PD9 RB501V-40

PR166 100K/F\_4

MAINON 29,30,34,35,36

Place this FB parts close to IC

21,30,31,34,36,37,38,40 +VIN

10,23,26,31,33,34,35,36,37,39,40 +5VS5

2,4,12,13,38 +1.5VSUS

12,13,36 +0.75V\_DDR\_VTT

+VIN\_DDR

PC249 0.1U/25V\_4  
PC243 4.7U/25V\_8  
PC251 4.7U/25V\_8

PL27 \*0.8/S

PC246 2200P/50V\_4

PC254 0.1U/25V\_4

PL26 NIMS0603-R82M

PR157 2.2\_8

PC127 2200P/50V\_4

PR163 \*0.2/S

PC236 390U/2.5V\_6X5.8ESR10

PC125 0.1U/10V\_4

Place this short pad close to output CAP

**+1.5VSUS +/- 5%**  
**Countinue current: 10A**  
**Peak current:12A**  
**OCp minimum 15A**

( 3mA )

4,12,13 DDR\_VTTREF

PC252 0.033U/10V\_4

V5FILT

PR159 \*0.4

PR268 0.4

PR162 0.4

8207S5

PR161 619K/F\_4

+VIN\_DDR

PR161 619K/F\_4

8207TON

PC140 0.1U/10V\_4

PD9 RB501V-40

PR166 100K/F\_4

MAINON 29,30,34,35,36

Place this FB parts close to IC

21,30,31,34,36,37,38,40 +VIN

10,23,26,31,33,34,35,36,37,39,40 +5VS5

2,4,12,13,38 +1.5VSUS

12,13,36 +0.75V\_DDR\_VTT


Place this short pad close to output CAP

Place this short pad close to output CAP

Place this short pad close to output CAP

Place this short pad close to output CAP

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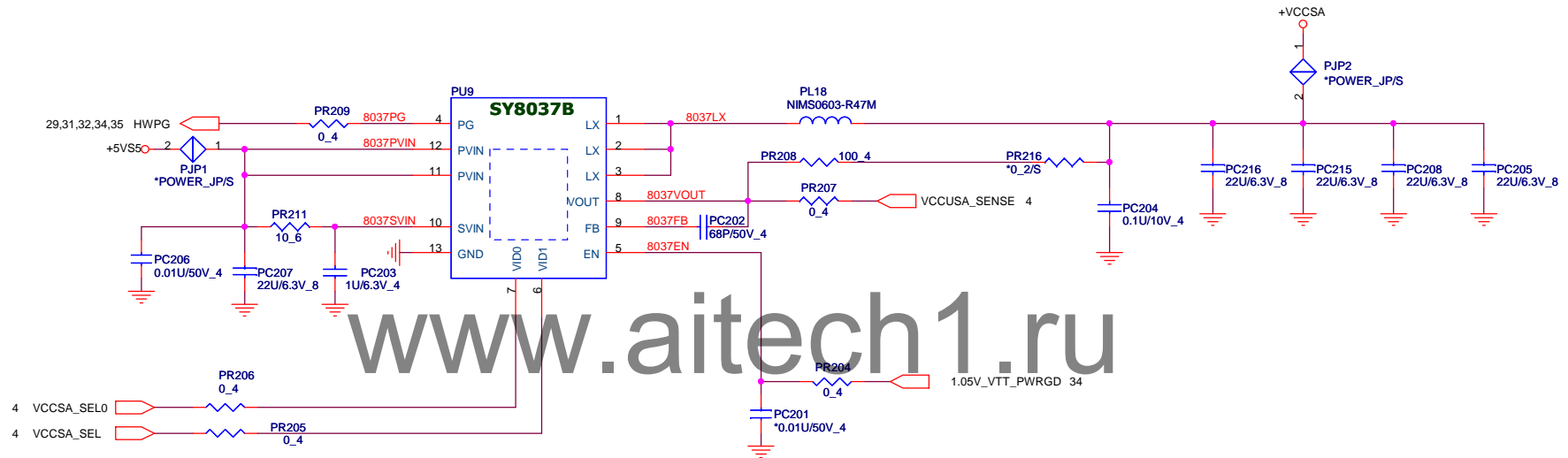
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**Quanta Computer Inc.**

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CPU system agent  
voltage slew rate of 0.5 -10 mV/ $\mu$ s

H_FC_C22 VID0	VCCSA_SEL VID1	Vout
0	0	0.9V
0	1	0.8V (SV)_(AL008037000_SY8037DCC) 0.85V (LV/ULV)_(AL008037001_SY8037ADCC)
1	0	0.725V
1	1	0.675V

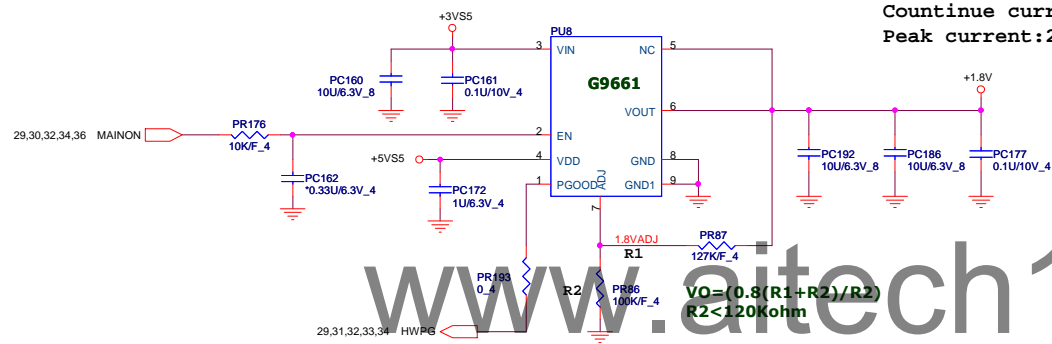
+VCCSA Volt +/- 5%  
Countinue current:4A  
Peak current:6A  
OCP minimum:7A



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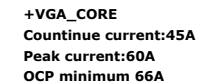








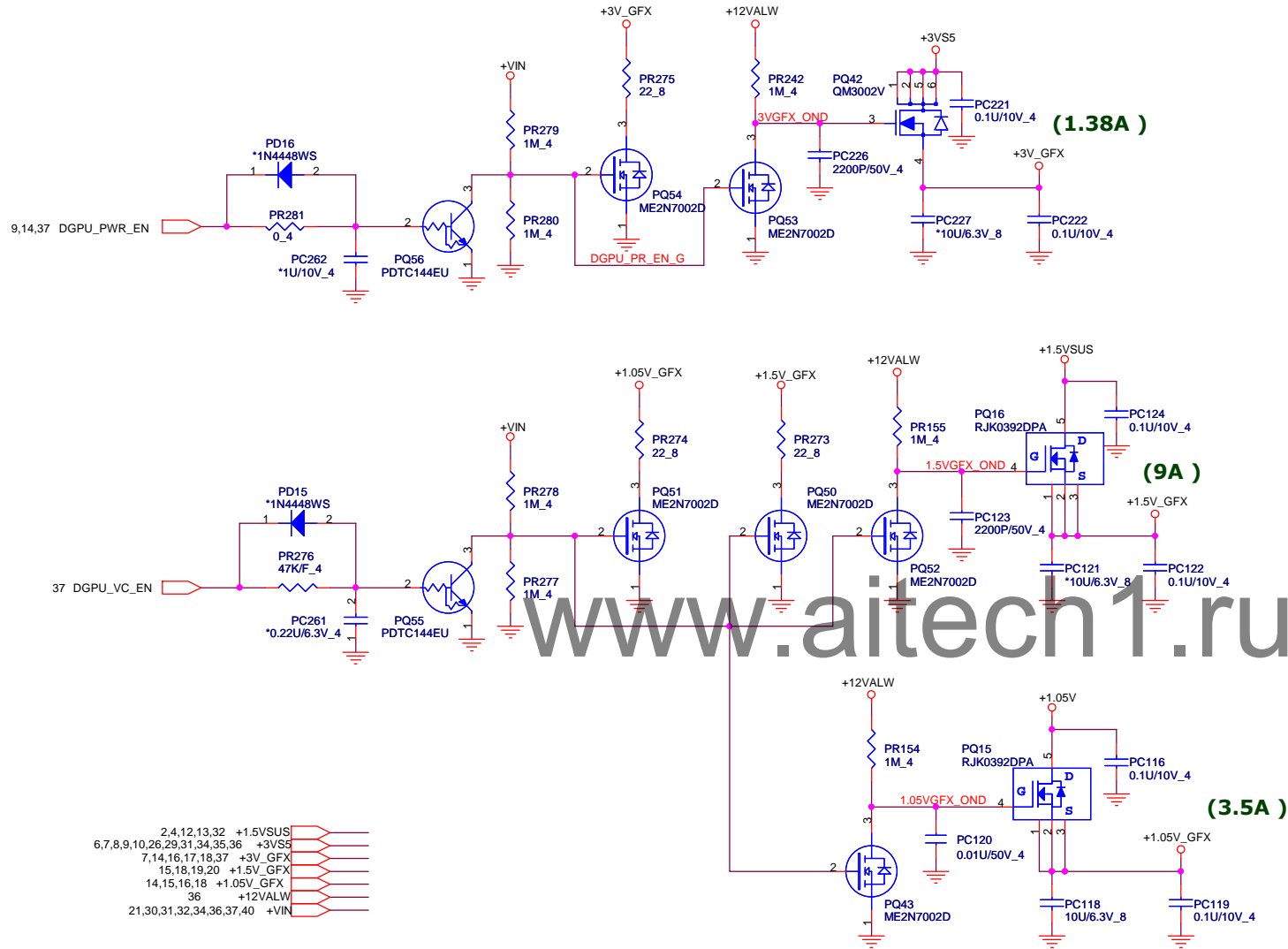
### Connect to input caps



### Shortest the

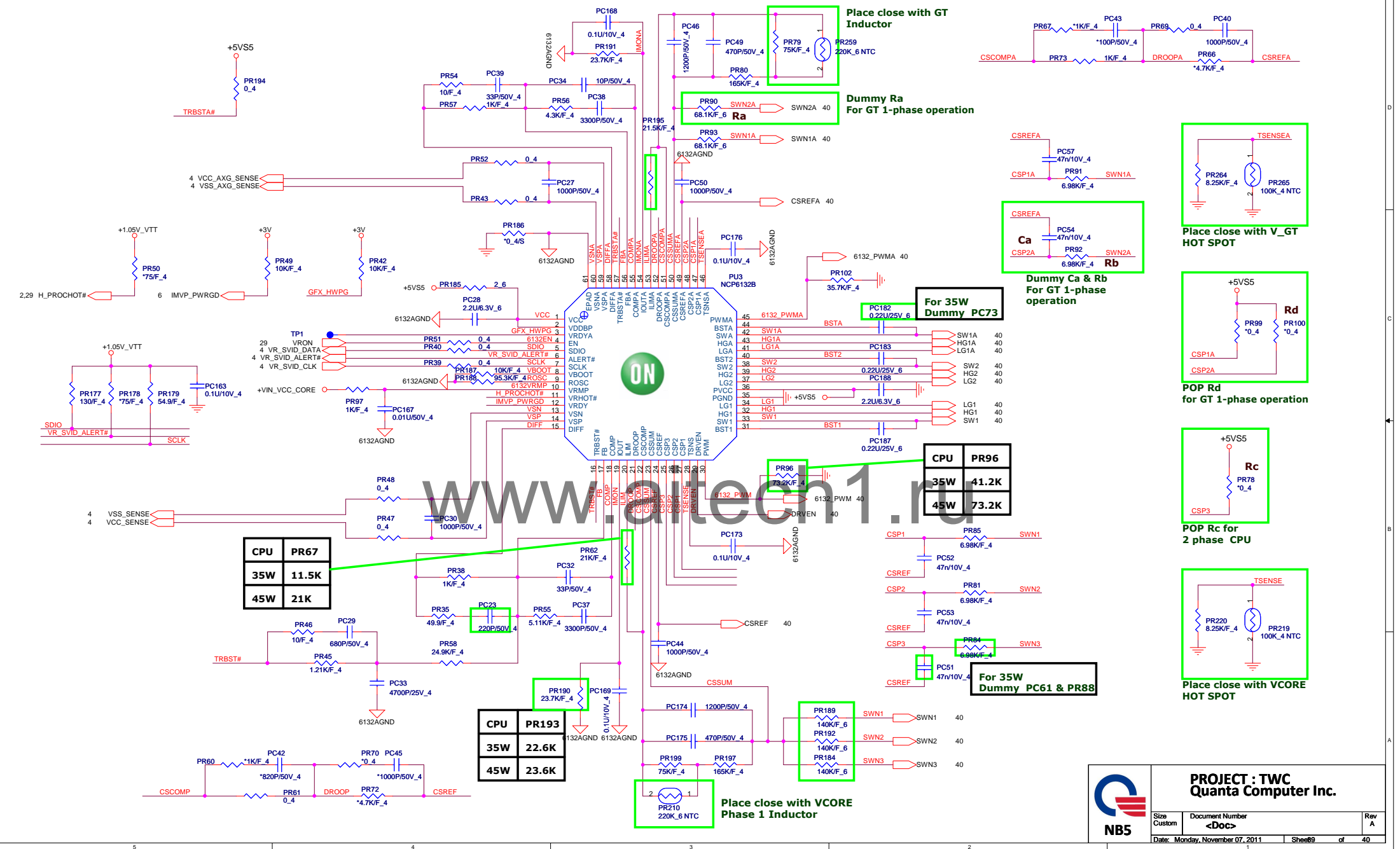
**Close to**

# VGA



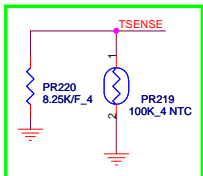
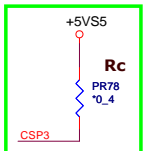
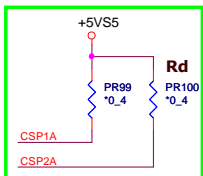
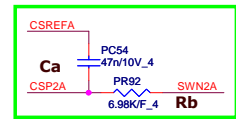
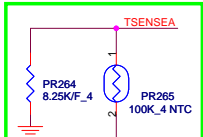
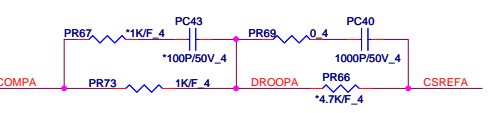
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Place close with GT Inductor

Dummy Ra For GT 1-phase operation




For 35W Dummy PC73

CPU	PR96
35W	41.2K
45W	73.2K

For 35W Dummy PC61 & PR88

CPU	PR193
35W	22.6K
45W	23.6K

Place close with VCORE Phase 1 Inductor



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